ABSTRACT

Design of clock data recovery IC for high speed data communication systems

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Demand for low cost Serializer and De-serializer (SerDes) integrated circuits has increased due to the widespread use of Synchronous Optical Network (SONET)/Gigabit Ethernet network and chip-to-chip interfaces such as PCI-Express (PCIe), Serial ATA(SATA) and Fibre channel standard applications. Among all these applications, clock data recovery (CDR) is one of the key design components. With the increasing demand for higher bandwidth and high integration, Complementary metal-oxidesemiconductor (CMOS) implementation is now a design trend for the predominant products. In this research work, a fully integrated 10Gb/s (OC-192) CDR architecture in standard 0.18 μ m CMOS is developed. The proposed architecture integrates the typically large off-chip filter capacitor by using two feed-forward paths configuration to generate the required zero and poles and satisfies SONET jitter requirements with a total power dissipation (including the buffers) of 290mW. The chip exceeds SONET OC-192 jitter tolerance mask, and high frequency jitter tolerance is over 0.31 UIpp by applying PRBS data with a pattern length of 231-1.The implementation is the first fully integrated 10Gb/s CDR IC which meets/exceeds the SONET standard in the literature. The second proposed CDR architecture includes an adaptive bang-bang control algorithm. For 6MHz sinusoidal jitter modulation, the new architecture reduces the tracking error to 11.4ps peak-to-peak, versus that of 19.7ps of the conventional bangbang CDR. The main contribution of the proposed architecture is that it optimizes the loop dynamics by adjusting the bang-bang bandwidth adaptively to minimize the steady state jitter of the CDR, which leads to an improved jitter tolerance performance. According to simulation, the jitter performance is improved by more than 0.04UI,which alleviates the stringent 0.1UI peak to peak jitter requirements in the PCIe/Fibre channel/Sonet Standard.