Blocker Tolerant Radio Architectures

ABSTRACT

Future radio platforms have to be inexpensive and deal with a variety of co-existence issues. The technology trend during the last few years is towards system on chip (SoC) that is able to process multiple standards re-using most of the digital and digitization resources. A major bottle-neck to this approach is the co-existence of this standards operating at different frequency bands that are hitting the antenna and receiver front-end. So the current research is focused on the optimization of various building blocks of the wireless transceivers for current and incoming standards.

The co-existence issue becomes more severe in broadband multi-standard receivers. Since the amount of out-of-band power is excessive compared with the desired channel, the linearity of both front-end and digitizer becomes the main limitation for achieving the required performance. This issue is even more relevant for cost effective saw-less architectures, where no or very weak RF filtering is present at the LNA input. SAW less radio front end is a cost effective and a possible solution for software defined radio (SDR). SDRs replace the multiple dedicated radios in a receiver with a single programmable radio, reducing, area, cost and power consumption. Non-linearities generate cross products and some of them are folded-back into the main channel increasing dramatically the in-band noise level.

The research work is devoted to the development of low cost, highly linear, inductorless RF front-ends, high performance radio partitioning methodology and blocker tolerant ADCs. During the research work on RF front ends, multiple linearization techniques for low noise amplifiers are developed. One proposed robust linearization technique is based on derivative

superposition method insensitive to P.V.T variations. The technique enhanced the linearity (IIP3) of LNAs by 10dB. Large signal linearity is also improved in another implementation. Highly linear LNAs are very critical for receivers especially for SAW less radio front ends.

During the research on blocker tolerant ADC architectures for wireless applications an intensive study and was done on the sensitivity of CT $\Delta\Sigma$ ADC to blockers jitter. Strong OOB blockers degrade the DR of the ADC and can potentially destabilize the system. A blocker tolerant CT $\Delta\Sigma$ ADC for broadband receivers is proposed. With the proposed integrated blocker detector/attenuator and minimally invasive integrated blocker filter, the implemented ADC achieves high blocker immunity.

A new radio partitioning technique presents a novel CMOS RF front end module (FEM) with Power amplifier (PA), Low noise amplifier (LNA) and Transmit/Receive (T/R) switch co-designed with Antenna. The co-design gives the many advantage and improves the overall performance. The architecture of this block called active antenna is separated from the SoC transceiver. This separated FEM design methodology gives robust analog and mixed signal radio development in scaled technology for SoC integration, and the co-design of the RF FEM-antenna system.

Patents:

1. **H. M. Geddada**, H. Xu, C.T. Fu and S. S. Taylor, 'A Transceiver with an integrated configurable passive network'

2. H. Xu, **H. M. Geddada** and C.T. Fu, 'Out-phasing power combination for power amplifiers'

Publications:

1. **H. M. Geddada**, C.J. Park, H.J. Jeon, J. Silva-Martinez, A.I. Karsilayan, "A blocker tolerant continuous-time $\Delta\Sigma$ ADC for Broadband Applications," *IEEE Transactions on VLSI systems* (*submitted*)

2. **H. M. Geddada**, C.T. Fu, J. Silva-Martinez and S. S. Taylor, "Wide-band, inductorless, low noise transconductance amplifiers with large signal linearity," *Transactions on Microwave Theory and Techniques, (submitted)*

3. J. Silva-Martinez, A. I. Karsilayan, **H. M. Geddada**, Blocker and Jitter Tolerant Wideband $\Sigma\Delta$ Modulators" *IEEE MWSCAS*, Idaho, Aug. 2012 (*Invited paper*)

4. C.J. Park, **H. M. Geddada**, M. Onabajo, A. I. Karsilayan, J. Silva-Martinez "A current-mode flash ADC for low power continuous-time sigma delta modulators," *ISCAS*, 2013

5. **H. M. Geddada**, J. Silva-Martinez, S. S. Taylor, 'Fully Balanced Low-Noise Transconductance Amplifiers with P1dB > 0 dBm in 45nm CMOS,' *IEEE European Solid-State Cir. Conf.*, Sept 2011

6. **H. M. Geddada**, J. Silva-Martinez, S. S. Taylor, 'Inductorless wideband CMOS LNAs with non-linearity cancellation,' *IEEE MWSCAS*. Conference, Seoul, Aug 2011 (***BEST STUDENT PAPER AWARD***)

7. J. Silva-Martinez, A. I. Karsilayan, **H. M. Geddada**, Aravind Padyana, C. J. Park, "A Blocker Tolerant Broadband Analog-to-Digital converter architecture" *Techcon conference, SRC*, Sep 2010.

8. **Geddada H. M**. ;Park, J.W.; Silva-Martinez, J. "Robust Derivative superposition Method for Linearizing Broadband LNA's" *IEE Electronics Letters* Vol. 45 Issue: 9 April 2009 (*Top 2nd paper accessed for the month of May 2009*).

9. Samanta, S.; Pam, S.; **Geddada, H.M**.; Mukhopadhyay, S. "An Improved Algorithm for Frequency Response Analysis of Switching Converters and its Implementation in Verilog-A" *ICIIS* Dec 2008.

VITA

Hemasundar Mohan Geddada was born in India. He received B.Tech. (Hons.) degree from Indian Institute of Technology (I.I.T.) Kharagpur, India in 2007 in Electrical Engineering. Since then he has been working towards the Ph.D. degree at the Department of Electrical and Computer Engineering, Texas A&M University, College Station, Texas. He was with Intel Corporation, Oregon during the summers of 2009, 2010 and 2011 as a graduate research intern. During his internship he worked on RF front end circuits on Intel's latest technologies that resulted in patents and publications. His Ph.D. program is sponsored by Semiconductor Research Corporation (SRC) from 2009 to 2012. His Ph.D. research covers blocker tolerant continuous time $\Delta\Sigma$ ADC, highly linear radio front end circuits and active antenna (CMOS front end module). He is the co-recipient of Best Student Paper award in 54th IEEE MWSCAS conference held in Seoul, Korea in 2011. He is the co-winner of the Analog IC design contest organized by several industries and held in Texas &M University, 2012. He can be reached by his email address ghsmohan@neo.tamu.edu.