ABSTRACT
Frequency Synthesis in Wireless and Wireline Systems. (December 2010)
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First, a frequency synthesizer for IEEE 802.15.4 / ZigBee transceiver applications that employs dynamic True Single Phase Clocking (TSPC) circuits in its frequency dividers is presented and through the analysis and measurement results of this synthesizer, the need for low power circuit techniques in frequency dividers is discussed.
Next, Differential Cascode Voltage-Switch-Logic (DCVSL) based delay cells are explored for implementing radio-frequency (RF) frequency dividers of low power frequency synthesizers. DCVSL flip-flops offer small input and clock capacitance which makes the power consumption of these circuits and their driving stages, very low. We perform a delay analysis of DCVSL circuits and propose a closed-form delay model that predicts the speed of DCVSL circuits with 8% worst case accuracy. The proposed delay model also demonstrates that DCVSL circuits suffer from a large low-to-high propagation delay (τ_{PLH}) which limits their speed and results in asymmetrical output waveforms. Our proposed enhanced DCVSL, which we call DCVSL-R, solves this delay bottleneck, reducing τ_{PLH} and achieving faster operation.
We implement two ring-oscillator-based voltage controlled oscillators (VCOs) in 0.13μm technology with DCVSL and DCVSL-R delay cells. In measurements, for the same oscillation frequency (2.4GHz) and same phase noise (-113dBc/Hz at 10MHz), DCVSL-R VCO consumes 30% less power than the DCVSL VCO. We also use the proposed DCVSL-R circuit to implement the 2.4GHz dual-modulus prescaler of a low power frequency synthesizer in 0.18μm technology. In measurements, the synthesizer exhibits -135dBc/Hz phase noise at 10MHz offset and 58μm settling time with 8.3mW power consumption, only 1.07mW of which is consumed by the dual modulus prescaler and the buffer that drives it. When compared to other dual modulus prescalers with similar division ratios and operating frequencies in literature, DCVSL-R dual modulus prescaler demonstrates the lowest power consumption.
An all digital phase locked loop (ADPLL) that operates for a wide range of frequencies to serve as a multi-protocol compatible PLL for microprocessor and serial link applications, is presented. The proposed ADPLL is truly digital and is implemented in a standard complementary metal-oxide-semiconductor (CMOS) technology without any analog/RF or non-scalable components. It addresses the challenges that come along with continuous wide range of operation such as stability and phase frequency detection for a large frequency error range. A proposed multi-bit bidirectional smart shifter serves as the digitally controlled oscillator (DCO) control and tunes the DCO frequency by turning on/off inverter units in a large row/column matrix that constitute the ring oscillator. The smart shifter block is completely digital, consisting of standard cell logic gates, and is capable of tracking the row/column unit availability of the DCO and shifting multiple bits per single update cycle. This enables fast frequency acquisition times without necessitating dual loop filter or gear shifting mechanisms.
The proposed ADPLL loop architecture does not employ costly, cumbersome

DACs or binary to thermometer converters and minimizes loop filter and DCO control complexity. The wide range ADPLL is implemented in 90nm digital CMOS technology and has a 9-bit TDC, the output of which is processed by a 10-bit digital loop filter and a 5-bit smart shifter. In measurements, the synthesizer achieves 2.5GHz-7.3GHz operation while consuming 10mW/GHz power, with an active area of 0.23 mm^2.