ABSTRACT

Threshold-Voltage Extraction Circuit. (August 2000)
Siew Kuok Hoon
B. Eng., National University of Singapore
Chair of Advisory Committee: Dr. Ugur Cilingiroglu

A novel optimally self-biasing MOSFET threshold-voltage (V_T) extractor circuit is presented. It implements the most popular industrial extraction algorithm of biasing a saturated MOSFET to the linear portion of its $\sqrt{I_D}$ versus V_{GS} characteristic, and extrapolating the tangential line to V_{GS} axis. The proposed circuit performs both tasks automatically in continuous time regardless of the dimensions and technology of the device under test. A simple feedback loop utilizing a differential difference amplifier (DDA) accomplishes auto biasing, while another DDA calculates the extrapolated value. The circuit is applicable to both NMOS and PMOS devices. The thesis presents the proposed extraction concept, describes the technique and circuit architecture, and verifies functionality by comparing simulated and experimental results with graphically extracted values. As a form of comparison, another V_T extraction circuit has been designed and fabricated. This circuit is similar to the majority of the published extractors but it alleviates some of the problems associated with them. Various circuit performance issues are investigated including power-supply variations and temperature dependence.