ABSTRACT

Reduced Area Discrete-Time Down-Sampling Filter Embedded With Windowed Integration Samplers

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Developing a flexible receiver, which can be reconfigured to multiple standards, is the key to solving the problem of embedding numerous and ever-changing functionalities in mobile handsets. Difficulty in efficiently reconfiguring analog blocks of a receiver chain to multiple standards calls for moving the ADC as close to the antenna as possible so that most of the processing is done in DSP. Different standards are sampled at different frequencies and a programmable anti-aliasing filtering is needed here. Windowed integration samplers have an inherent sinc filtering which creates nulls at multiples of fs. The attenuation provided by sinc filtering for a bandwidth B is directly proportional to the sampling frequency fs and, in order to meet the anti-aliasing specifications, a high sampling rate is needed. ADCs operating at such a high oversampling rate dissipate power for no good use. Hence, there is a need to develop a programmable discrete-time down-sampling circuit with high inherent anti-aliasing capabilities. Currently existing topologies use large numbers of switches and capacitors which occupy a lot of area.A novel technique in reducing die area on a discrete-time sinc2 $\downarrow 2$ filter for charge sampling is proposed. An SNR comparison of the conventional and the proposed topology reveals that the new technique saves 25 percent die area occupied by the sampling capacitors of the filter. The proposed idea is also extended to implement higher downsampling factors and a greater percentage of area is saved as the down-sampling factor is increased. The proposed filter also has the topological advantage over previously reported works of allowing the designers to use active integration to charge the capacitance, which is critical in obtaining high linearity. A novel technique to implement a discrete-time sinc3 $\downarrow 2$ filter for windowed integration samplers is also proposed. The topology reduces the idle time of the integration capacitors at the expense of a small complexity overhead in the clock generation, thereby saving 33 percent of the die area on the capacitors compared to the currently existing topology. Circuit Level simulations in 45 nm CMOS technlogy show a good agreement with the predicted behaviour obtained from the analaysis.