ABSTRACT

A 3-Bit Current Mode Quantizer for Continuous Time Delta Sigma Analog-to-Digital Converters

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The summing amplifier and the quantizer form two of the most critical blocks in a continuous time delta sigma (CT ΔΣ) analog-to-digital converter (ADC). Most of the conventional CT ΔΣ ADC designs incorporate a voltage summing amplifier and a voltage-mode quantizer. The high gain-bandwidth (GBW) requirement of the voltage summing amplifier increases the overall power consumption of the CT ΔΣ ADC. In this work, a novel method of performing the operations of summing and quantization is proposed. A current-mode summing stage is proposed in the place of a voltage summing amplifier. The summed signal, which is available in current domain, is then quantized with a 3-bit current mode flash ADC. This current mode summing approach offers considerable power reduction of about 80% compared to conventional solutions [2]. The total static power consumption of the summing stage and the quantizer is 5.3mW. The circuits were designed in IBM 90nm process. The static and dynamic characteristics of the quantizer are analyzed. The impact of process and temperature variation and mismatch tolerance as well as the impact of jitter, in the presence of an out-of-band blocker signal, on the performance of the quantizer is also studied.