Title

Design of Analog & Mixed Signal Circuits in Continuous-Time Sigma-Delta Modulators for System-on-Chip Applications

Abstract

Software-defined radio receivers (SDRs) have become popular to accommodate multi-standard wireless services using a single chip-set solution in mobile telecommunication systems. In SDRs, the signal is down-converted to an intermediate frequency and then digitalized. This approach relaxes the specifications for most of the analog front-end building blocks by performing most of the signal processing in the digital domain. However, since the analog-to-digital converter (ADC) is located as close as possible to the antenna in SDR architectures, the ADC specification requirements are very stringent because a large amount of interference signals are present at the ADC input due to the removal of filtering blocks, which particularly affects the dynamic range (DR) specification. Sigma-delta (ΣΔ) ADCs have several benefits such as low implementation cost, especially when the architecture contains mostly digital circuits. Furthermore, continuous-time (CT) ΣΔ ADCs allow to eliminate the anti-aliasing filter because input signals are sampled after the integrator. The bandwidth requirements for the amplifiers in CT ΣΔ ADCs can be relaxed due to the continuous operation without stringing settling time requirements. Therefore, they are suitable for high-speed and low-power applications. In addition, CT ΣΔ ADCs achieve high resolution due to the ΣΔ modulator's noise shaping property. However, the in-band quantization noise is shaped by the analog loop filter and the distortions of the analog loop filter directly affect the system output. Hence, highly linear low-noise loop filters are required for high-performance ΣΔ modulators.

First, a 5^{th}–order active-RC loop filter with a cutoff frequency of 20MHz for a low pass (LP) CT ΣΔ modulator was designed and fabricated in CMOS 90nm technology as part of this dissertation research. The active-RC topology is selected because of the high DR requirement in SDR applications. The amplifiers in the first stage of the loop filter are implemented with linearization techniques employing anti-parallel cancellation and source degeneration in the second stage of the amplifiers. These techniques improve the third-order intermodulation (IM3) by approximately 10dB; while noise, area, and power consumption do not increase by more than 10%. Second, a current-mode adder-flash ADC was also fabricated as part of a LP CT ΣΔ modulator. The proposed current-mode operation leads to a 50% power reduction and lessens existing problems associated with voltage-mode flash ADCs, which are mainly related to voltage headroom restrictions, speed of operation, offsets, and power efficiency of the latches. The core of the current-mode adder-flash ADC was fabricated in CMOS 90nm technology with 1.2V supply, and it dissipates 3.34mW while operating at 1.48GHz and consuming a die area of $0.0276mm^2$.

System-on chip (SoC) solutions are becoming more popular in mobile telecommunication systems to improve the portability and competitiveness of products. Since the analog/RF and digital blocks often share the same external power supply in SoC solutions, the on-chip generation of clean power supplies is necessary to avoid system performance degradation due to supply noises. Finally, the critical design issues for external capacitor-less low drop-out (LDO) regulators for SoC applications are addressed in this dissertation, especially the challenges related to power supply rejection at high frequencies as well as loop stability and transient response. The paths of the power supply noise to the LDO output were analyzed, and a power supply noise cancellation circuit has been developed. The power supply rejection (PSR) performance has been improved by using a replica circuit that tracks the main supply noise under process-voltage-temperature variations and all operating conditions. Fabricated in a 0.18μm CMOS technology with 1.8V supply, the entire proposed LDO consumes 55μA of quiescent current while in standby operation, and it has a drop-out voltage of 200mV when providing 50mA to the load. Its active core chip area is $0.14mm^2$. Compared to a conventional uncompensated LDO, the proposed architecture presents a PSR improvement of 34dB and 25dB at 1MHz and 4MHz, respectively.