High-speed and low resolution analog-to-digital converters (ADC) are key elements in the read channel of optical and magnetic data storage systems. The required resolution is about 6-7 bits while the sampling rate and effective resolution bandwidth requirements with each generation of storage system. Folding is a technique to reduce the increase number of comparators used in the flash architecture. By means of an analog preprocessing circuit in folding A/D converters the number of comparators can be reduced significantly. Folding architectures exhibit low power and low latency as well as the ability to run at high sampling rates. Folding ADCs employing interpolation schemes to generate extra folding waveforms are called "Folding and Interpolating ADC" (F&I ADC).

The aim of this research is to increase the input bandwidth of high speed conversion, and low latency F&I ADC. Behavioral models are developed to analyze the bandwidth limitation at the architecture level. A front-end sample-and-hold unit is employed to tackle the frequency multiplication problem, which is intrinsic for all F&I ADCs. Current-mode signal processing is adopted to increase the bandwidth of the folding amplifiers and interpolators, which are the bottleneck of the whole system. An operational transconductance amplifier (OTA) based folding amplifier, current mirror-based interpolator, very low impedance fast current comparator are proposed and designed to carry out the current-mode signal processing. A new bit synchronization scheme is proposed to correct the error caused by the delay difference between the coarse and fine channels.

A prototype chip was designed and fabricated in 0.35μm CMOS process to verify the ideas. The S/H and F&I ADC prototype is realized in 0.35μm double-poly CMOS process (only one poly is used). Integral nonlinearity (INL) is 1.0 LSB and Differential nonlinearity (DNL) is 0.6 LSB at 110 KHz. The ADC occupies 1.2mm2 active area and dissipates 200mW (excluding 70mW of S/H) from 3.3V supply. At 300MSPS sampling rate, the ADC achieves no less than 6 ENOB with input signal lower than 60MHz. It has the highest input bandwidth of 60MHz reported in the literature for this type of CMOS ADC with similar resolution and sample rate.