ABSTRACT

High Performance Building Blocks for Wireless Receiver:

Multi-Stage Amplifiers and Low Noise Amplifiers. (December 2007)

Xiaohua Fan, B.S., Tsinghua University;

M.S., Chinese Academy of Sciences

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Different wireless communication systems utilizing different standards and for multiple applications have penetrated the normal people's life, such as Cell phone, Wireless LAN, Bluetooth, Ultra wideband (UWB) and WiMAX systems. The wireless receiver normally serves as the primary part of the system, which heavily influences the system performance. This research concentrates on the designs of several important blocks of the receiver; multi-stage amplifier and low noise amplifier.

Two novel multi-stage amplifier typologies are proposed to improve the bandwidth and reduce the silicon area for the application where a large capacitive load exists. They were designed using AMI 0.5 μm CMOS technology. The simulation and measurement results show they have the best Figure-of-Merits (FOMs) in terms of small signal and large signal performances, with 4.6MHz and 9MHz bandwidth while consuming 0.38mW and 0.4mW power from a 2V power supply.

Two Low Noise Amplifiers (LNAs) are proposed, with one designed for narrowband application and the other for UWB application. A noise reduction technique is proposed

for the differential cascode Common Source LNA (CS-LNA), which reduces the LNA Noise Figure (NF), increases the LNA gain, and improves the LNA linearity. At the same time, a novel Common Gate LNA (CG-LNA) is proposed for UWB application, which has better linearity, lower power consumption, and reasonable noise performance.

Finally a novel practical current injection built-in-test (BIT) technique is proposed for the RF Front-end circuits. If the off-chip component Lg and Rs values are well controlled, the proposed technique can estimate the voltage gain of the LNA with less than 1dB (8%) error.