ABSTRACT

Design and Implementation of CMOS Radio Frequency Receivers. (May 2002)

Wenjun Sheng, B.S., Tsinghua University, China;

M.E., Texas A&M University

Chairs of Advisory Committee: Dr. Edgar Sánchez-Sinencio

The rapidly growing wireless communication market creates a high demand for radio frequency (RF) transceivers. Low-cost, low-power, and small form fact are the essential requirements for modern RF receivers. To accomplish a successful design meeting all these requirements, not only advanced process technology and circuit design techniques are vital, but also a breakthrough on system level, both the system level design methodology and receiver architecture, is necessary.

In this dissertation, system level design techniques are explored to generate optimized RF system designs. A system design methodology is proposed to accomplish a RF system design starting from wireless communication standards. New techniques that are suitable to analyze highly integrated systems are provided. For the first time in the literature, we propose a method to rationally distribute system specifications among the building blocks of a RF receiver. The proposed approach is formulated to yield a minimum power consumption of the receiver. A CMOS receiver for Bluetooth application is designed to demonstrate the methodology. The receiver is implemented with a low cost, main stream 0.35mm CMOS technology. To enable a cheap, low power solution, this work develops a receiver architecture that lends itself to complete integration. The Bluetooth receiver chip has been fabricated and tested. The entire system includes the RF front end, frequency synthesizer and baseband blocks. It consumes 65mA current from a 3V power supply. The measured performance of 82dBm sensitivity is the best up to date comparing with published industry solutions implemented with more expensive RF-CMOS technologies.

As part of the Bluetooth receiver design, a CMOS low noise amplifier (LNA) working at 2.4GHz is designed. A complete noise modeling of MOSFETs enables the realization of a sub-3dB noise figure differential LNA with only 4.5mA current from a 3V power supply. A mixed mode GFSK demodulator that is low power, low-cost and achieves a performance very close to the optimum correlator is also proposed.

Another contribution is at the system level design of a multi-standard receiver for 3G applications. A receiver architecture suitable for multi-standard application is proposed. Circuit specifications of key building blocks in the receiver are provided.