ABSTRACT

Baseband analog circuits in deep-submicron cmos technologies targeted for mobile multimedia

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Three main analog circuit building blocks that are important for a mixed-signal system are investigated in this work. New building blocks with emphasis on power efficiency and compatibility with deep-submicron technology are proposed and experimental results from prototype integrated circuits are presented. Firstly, a 1.1GHz, 5th order, active-LC, Butterworth wideband equalizer that controls inter-symbol interference and provides anti-alias filtering for the subsequent analog to digital converter is presented. The equalizer design is based on a new series LC resonator biquad whose power efficiency is analytically shown to be better than a conventional Gm-C biquad. A prototype equalizer is fabricated in a standard 0.18μm CMOS technology. It is experimentally verified to achieve an equalization gain programmable over a 0-23dB range, 47dB SNR and -48dB IM3 while consuming 72mW of power. This corresponds to more than 7 times improvement in power efficiency over conventional Gm-C equalizers. Secondly, a load capacitance aware compensation for 3-stage amplifiers is presented. A class-AB 16W headphone driver designed using this scheme in 130nm technology is experimentally shown to handle 1pF to 22nF capacitive load while consuming as low as 1.2mW of quiescent power. It can deliver a maximum RMS power of 20mW to the load with -84.8dB THD and 92dB peak SNR, and it occupies a small area of 0.1mm2. The power consumption is reduced by about 10 times compared to drivers that can support such a wide range of capacitive loads. Thirdly, a novel approach to design of ADC in deep-submicron technology is described. The presented technique enables the usage of time-to-digital converter (TDC) in a delta-sigma modulator in a manner that takes advantage of its high timing precision while noise-shaping the error due to its limited time resolution. A prototype ADC designed based on this deep-submicron technology friendly architecture was fabricated in a 65nm digital CMOS technology. The ADC is experimentally shown to achieve 68dB dynamic range in 20MHz signal bandwidth while consuming 10.5mW of power. It is projected to reduce power and improve speed with technology scaling.