ABSTRACT

Design of High Performance Frequency Synthesizers
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Sung Tae Moon, B.S., Seoul National University
Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Frequency synthesizer is a key building block of fully-integrated wireless communication systems. Design of a frequency synthesizer requires the understanding of not only the circuit-level but also of the transceiver system-level considerations. This dissertation presents a full cycle of the synthesizer design procedure starting from the interpretation of standards to the testing and measurement results.

A new methodology of interpreting communication standards into low level circuit specifications is developed to clarify how the requirements are calculated. A detailed procedure to determine important design variables is presented incorporating the fundamental theory and non-ideal effects such as phase noise and reference spurs. The design procedure can be easily adopted for different applications.

A BiCMOS frequency synthesizer compliant for both wireless local area network (WLAN) 802.11a and 802.11b standards is presented as a design example. The two standards are carefully studied according to the proposed standard interpretation method. In order to satisfy stringent requirements due to the multi-standard architecture, an improved adaptive dual-loop phase-locked loop (PLL) architecture is proposed. The proposed improvements include a new loop filter topology with an active capacitance multiplier and a tunable dead zone circuit. These improvements are crucial for monolithic integration of the synthesizer with no off-chip components.

The proposed architecture extends the operation limit of conventional integer-

N type synthesizers by providing better reference spur rejection and settling time performance while making it more suitable for monolithic integration. It opens a new possibility of using an integer-N architecture for various other communication standards, while maintaining the benefit of the integer-N architecture; an optimal performance in area and power consumption.