Baseband Continous-Time Sigma-Delta analog-to-Digital Conversion for ADSL Applications

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Almost all earlier high speed ΣΔ modulators with MHz signal bandwidth are implemented with SC (switched -capacitor) circuit techniques. Whereas ΣΔ modulators with continuous -time loop filters have the advantages of lower power consumption and intrinsic anti -alias filtering. Moreover, because the sampler of a continuous -time ΣΔ modulator is right in front of the quantizer inside of the noise shaping loop, any sampling error at signal frequencies is greatly suppressed by the high gain of the loop filter together with the quantization noise. Thus key non -idealities associated with the front -end sampling network in SC modulators are avoided. Prior implementations of continuous-time ΣΔ modulators in CMOS have either narrow bandwidth (200 -kHz bandwidth with 82-dB dynamic range) or limited dynamic range (2-MHz bandwidth with 70-dB dynamic range) due to architecture level limitations.

This dissertation presents the design and experimental results of an 88 -dB dynamic range 1.1-MHz input signal bandwidth continuous -time ΣΔ modulator for ADSL applications. The proposed ΣΔ modulator architecture and circuit design techniques can be easily applied to other wireless or wireline communication applications. Highlights of the proposed architecture include: i) Multi -bit quantiz ation is employed to significantly improve resolution and bandwidth. ii) NRZ (Non -Return-to-Zero) feedback DAC pulse shaping and multi -bit quantization are utilized to effectively reduce clock jitter sensitivity. iii) Excess loop delay problem of conventional continuous -time ΣΔ modulators is eliminated. iv) A sound continuous -time noise shaping loop filter design with discrete-tunable capacitors achieves a high and stable SNR over large (such as ± 50%) process variations supply. Our work improves signal bandwidth by 5.5 and 11 times compared with prior publications with similar dynamic range performance. Clock jitter sensitivity is reduced by more than 33 dB over prior work as simulated and calculated.