

Abstract

Design of CMOS integrated phase-locked loops for multi-gigabits serial data links
(Dec 2006)

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High-speed serial data links are quickly gaining in popularity and replacing the conventional parallel data links in recent years when the data rate of communication exceeds one gigabits per second. Compared with parallel data links, serial data links are able to achieve higher data rate and longer transfer distance. This dissertation is focused on the design of CMOS integrated phase-locked loops (PLLs) and relevant building blocks used in multi-gigabits serial data link transceivers. Firstly, binary phase-locked loops (BPLLs, i.e., PLLs based on binary phase detectors) are modeled and analyzed. The steady-state behavior of BPLLs is derived with combined discrete-time and continuous-time analysis. The jitter performance characteristics of BPLLs are analyzed. Secondly, a 10 Gbps clock and data recovery (CDR) chip for SONET OC-192, the mainstream standard for optical serial data links, is presented. The CDR is based on a novel referenceless dual-loop half-rate architecture. It includes a binary phase-locked loop based on a quad-level phase detector and a linear frequency-locked loop based on a linear frequency detector. The proposed architecture enables the CDR to achieve large locking range and small jitter generation at the same time. The prototype is implemented in 0.18 μm CMOS technology and consumes 250 mW under 1.8 V supply. The jitter generation is 0.5 ps-rms and 4.8 ps-pp. The jitter peaking and jitter tolerance performance exceeds the specifications defined by SONET OC-192 standard. Thirdly, a fully-differential divide-by-eight injection-locked frequency divider with low power dissipation is presented. The frequency divider consists of a four-stage ring of CML (current mode logic) latches. It has a maximum operating frequency of 18 GHz. The ratio of locking range over center frequency is up to 50%. The prototype chip is implemented in 0.18 μm CMOS technology and consumes 3.6 mW under 1.8 V supply. Lastly, the design and optimization techniques of fully differential charge pumps are discussed. Techniques are proposed to minimize the nonidealities associated with a fully differential charge pump, including differential mismatch, output current variation, low-speed glitches and high-speed glitches. The performance improvement brought by the techniques is verified with simulations of schematics designed in 0.35 μm CMOS technology.