ABSTRACT

Oscillator Architectures and Enhanced Frequency Synthesizer. (December 2009)

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A voltage controlled oscillator (VCO) that generates a periodic signal whose frequency is tuned by a voltage is a key building block in any integrated circuit system. A sine wave oscillator can be used for a built-in self testing where high linearity is required. A bandpass filter (BPF) based oscillator is a preferred solution, and high quality factor (Q-factor) is needed to improve the linearity. However, a stringent linearity specification may require very high Q-factor, and is not practical to implement. To address this problem, a frequency harmonic shaping technique is proposed. It utilizes a finite impulse response filter improving the linearity by rejecting certain harmonics. A prototype SC BPF oscillator with an oscillating frequency of 10 MHz is designed and measurement results show that linearity is improved by 20 dB over a conventional oscillator.

In radio frequency area, preferred oscillator structures are an LC oscillator and a ring oscillator. An LC oscillator exhibits good phase noise but an expensive cost of an inductor is disadvantageous. A ring oscillator can be built in standard CMOS process, but suffers due to a poor phase noise and is sensitive to supply noise. An RC BPF

oscillator is proposed to compromise the above difficulties. An RC BPF oscillator at 2.5 GHz is designed and measured performance is better than ring oscillators when compared using a figure of merit. In particular, the frequency tuning range of the proposed oscillator is superior to the ring oscillator.

VCO is normally incorporated with a frequency synthesizer (FS) for an accurate frequency control. In an integer-N FS, reference spur is one of the design concerns in communication systems since it degrades a signal to noise ratio. Reference spurs can be rejected more by either the lower loop bandwidth or the higher loop filter. But the former increases a settling time and the latter decreases phase margin. An adaptive lowpass filtering technique is proposed. The loop filter order is adaptively increased after the loop is locked. A 5.8 GHz integer-N FS is designed and measurement results show that reference spur rejection is improved by 20 dB over a conventional FS without degrading the settling time. A new pulse interleaving technique is proposed and several design modifications are suggested as a future work.