ABSTRACT

Design Techniques for High Speed Low Voltage and Low Power Non-Calibrated Pipeline Analog to Digital Converters

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The profound digitization of modern microelectronic modules made Analog-to- Digital converters (ADC) key components in many systems. With resolutions up to 14bits and sampling rates in the 100s of MHz, the pipeline ADC is a prime candidate for a wide range of applications such as instrumentation, communications and consumer electronics. However, while past work focused on enhancing the performance of the pipeline ADC from an architectural standpoint, little has been done to individually address its fundamental building blocks. This work aims to achieve the latter by proposing design techniques to improve the performance of these blocks with minimal power consumption in low voltage environments, such that collectively high performance is achieved in the pipeline ADC. Towards this goal, a Recycling Folded Cascode (RFC) amplifier is proposed as an enhancement to the general performance of the conventional folded cascode. Tested in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18?m Complementary Metal Oxide Semiconductor (CMOS) technology, the RFC provides twice the bandwidth, 8-10dB additional gain, more than twice the slew rate and improved noise performance over the conventional folded cascode-all at no additional power or silicon area. The direct auto-zeroing offset cancellation scheme is optimized for low voltage environments using a dual level common mode feedback (CMFB) circuit, and amplifier differential offsets up to 50mV are effectively cancelled. Together with the RFC, the dual level CMFB was used to implement a sample and hold amplifier driving a singleended load of 1.4pF and using only 2.6mA; at 200MS/s better than 9bit linearity is achieved. Finally a power conscious technique is proposed to reduce the kickback noise of dynamic comparators without resorting to the use of pre-amplifiers. When all techniques are collectively used to implement a 1Vpp 10bit 160MS/s pipeline ADC in Semiconductor Manufacturing International Corporation (SMIC) 0.18[mu]m CMOS, 9.2 effective number of bits (ENOB) is achieved with a near Nyquist-rate full scale signal. The ADC uses an area of 1.1mm2 and consumes 42mW in its analog core. Compared to recent state-of-the-art implementations in the 100-200MS/s range, the presented pipeline ADC uses the least power per conversion rated at 0.45pJ/conversion-step.