# ABSTRACT


Jitter-Tolerance and Blocker-Tolerance of ΔΣ Analog-to-Digital Converters for SAW-Less Multi-Standard Receivers. (August 2012)

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The quest for multi-standard and software-defined radio receivers (SDR) receivers calls for high flexibility and reconfigurability in the receiver building-blocks so that to accommodate several wireless services using a single receiver chain in mobile handsets. A potential approach to achieve flexibility in the receiver is to move the analog-to-digital converter (ADC) closer to the antenna so that to exploit the enormous advances in digital signal processing (DSP), in terms of technology scaling, speed, and programmability. However, as the ADC moves closer to the antenna, several blockers and interferers are present at the ADC input. In this context, continuous-time (CT) delta-sigma (ΔΣ) ADCs show up as an attractive option. CT ΔΣ ADCs have gained significant attention in wideband receivers, because of their amenability to operate at a higher-speed with lower power consumption compared to discrete-time (DT) implementations, inherent anti-aliasing, and robustness to sampling errors in the quantizer. However, CT ΔΣ modulators suffer from a critical limitation due to their high sensitivity to the clock-jitter in the feedback digital-to-analog converter (DAC) sampling-clock. Also, it is important to investigate the sensitivities of CT ΔΣ ADCs to out-of-band (OOB) blockers at the ADC input and find the design considerations that should be taken into account and develop convenient solutions if needed so that to make the performance of CT ΔΣ modulators tolerant to OOB blockers showing up at the ADC input. Recall that the introduction of multi-standard wireless terminals and SDRs will motivate the expansion of the wireless market and services, making the wireless environment even more hostile.

A simple hybrid DAC solution for CT ΔΣ modulators is presented that achieves tolerance to DAC pulse-width jitter (PWJ) errors by spectrally shaping the jitter induced errors. The proposed technique features an effecient combination between the conventional rectangular-pulse switched-current (SI) DAC and a DT switched-capacitor-resistor (SCR) DAC to achieve spectral shaping for the jitter induced error in the modulator's feedback signal. To demosntrate the potential of the proposed solution, a 384 MHz second-order single-bit CT ΔΣ modulator for WCDMA baseband channel of 1.92 MHz has been designed using the proposed feedback hybrid DAC structure. The ΔΣ modulator is implemented in a 1.2 V, 90nm, IBM 9LP CMOS process. A maximum signal-to-noise-plus-distortion ratio (SNDR) of 68 dB over a 1.92 MHz bandwidth is achieved, while consuming 3.44 mW. Results show 26 dB robustness to PWJ over the commonly used non-return-to-zero (NRZ) DACs.

The sensitivity of ΔΣ modulators with CT loop filters to DAC PWJ in presence of blockers has been investigated in details. The developed analysis covers the commonly used DAC types including SI RZ, SI NRZ, and SCR with exponentially-decaying waveform. It has been shown that for all types of multi-bit DACs, the IBJN induced by a blocker signal increases proportionally with the power of the blocker component in the feedback path and also varies periodically with the blocker frequency through a squared sinusoidal factor for multi-bit NRZ DACs. Also, the performance limitations due to nonlinearities in the loop filter are studied. It is shown that the most critical problem caused by OOB blockers is the noise folding due to nonlinearity at the input stage of the loop filter. Particulalrly, in presence of a $6\ dBFS$ OOB blocker, noise folding at the first integrator stage, with $IIP_3 = 23\ dBFS$, can significantly deteriorate the ADC sensitivity by 30 dB, turning weak desired signals undetectable. Furthermore, in presence of large OOB blockers, the noise folding problem raises the $IIP_3$ requirement on the first stage in the loop filter to extremely high values ($\sim 39\ dBFS$). A potential solution is proposed to alleviate the sensitivity to noise folding through current-mode integration at the ADC input stage.