ABSTRACT

Analog Baseband Filters and Mixed Signal Circuits for Broadband Receiver Systems

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Data transfer rates of communication systems continue to rise fueled by aggressive demand for voice, video and Internet data. Device scaling enabled by modern lithography has paved way for System-on-Chip solutions integrating compute intensive digital signal processing. This trend coupled with demand for low power, battery-operated consumer devices offers extensive research opportunities in analog and mixed-signal designs that enable modern communication systems. The first part of the research deals with broadband wireless receivers. With an objective to gain insight, we quantify the impact of undesired out-band blockers on analog baseband in a broadband radio. We present a systematic evaluation of the dynamic range requirements at the baseband and A/D conversion boundary. A prototype UHF receiver designed using RFCMOS 0.18?m technology to support this research integrates a hybrid continuous- and discrete-time analog baseband along with the RF front-end. The chip consumes 120mW from a 1.8V/2.5V dual supply and achieves a noise figure of 7.9dB, an IIP3 of -8dBm (+2dbm) at maximum gain (at 9dB RF attenuation). High linearity active RC filters are indispensable in wireless radios. A novel feed-forward OTA applicable to active RC filters in analog baseband is presented. Simulation results from the chip prototype designed in RFCMOS 0.18um technology show an improvement in the out-band linearity performance that translates to increased dynamic range in the presence of strong adjacent blockers. The second part of the research presents an adaptive clock-recovery system suitable for high-speed wireline transceivers. The main objective is to improve the jitter-tracking and jitter-filtering trade-off in serial link clock-recovery applications. A digital state-machine that enables the proposed mixed-signal adaptation solution to achieve this objective is presented. The advantages of the proposed mixed-signal solution operating at 10Gb/s are supported by experimental results from the prototype in RFCMOS 0.18?m technology.