ABSTRACT

Frequency Synthesizers and Oscillator Architectures
Based on Multi-Order Harmonic Generation (December 2011)
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Frequency synthesizers are essential components for modern wireless and wireline communication systems as they provide the local oscillator signal required to transmit and receive data at very high rates. They are also vital for computing devices and microcontrollers as they generate the clocks required to run all the digital circuitry responsible for the high speed computations. Data rates and clocking speeds are continuously increasing to accommodate for the ever growing demand on data and computational power. This places stringent requirements on the performance metrics of frequency synthesizers. They are required to run at higher speeds, cover a wide range of frequencies, provide a low jitter/phase noise output and consume minimum power and area. In this work, we present new techniques and architectures for implementing high speed frequency synthesizers which fulfill the aforementioned requirements. We propose a new architecture and design approach for the realization of wideband millimeter-wave frequency synthesizers. This architecture uses two-step multi-order harmonic generation of a low frequency phase-locked signal to generate wideband mm-wave frequencies. A prototype of the proposed system is designed and fabricated in 90nm Complementary Metal Oxide Semiconductor (CMOS) technology. Measurement results demonstrated that a very wide tuning range of 5 to 32 GHz can be achieved, which is costly to implement using conventional techniques. Moreover the power consumption per octave resembles that of state-of-the art reports. Next, we propose the N-Push cyclic coupled ring oscillator (CCRO) architecture to implement two high performance oscillators: (1) a wideband N-Push/M-Push CCRO operating from 3.16-12.8GHz implemented by two harmonic generation operations using the availability of different phases from the CCRO, and (2) a 13-25GHz millimeter-wave N-Push CCRO with a low phase noise performance of -118dBc/Hz at 10MHz. The proposed oscillators achieve low phase noise with higher FOM than state of the art work. Finally, we present some improvement techniques applied to the performance of phase locked loops (PLLs). We present an adaptive low pass filtering technique which can reduce the reference spur of integer-N charge-pump based PLLs by around 20dB while maintaining the settling time of the original PLL. Another PLL is presented, which features very low power consumption targeting the Medical Implantable Communication Standard. It operates at 402-405 MHz while consuming 600microW from a 1V supply.