ABSTRACT

High performance CMOS integrated circuits for optical receivers

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Optical communications is expanding into new applications such as infrared wireless communications; therefore, designing high performance circuits has gained considerable importance. In this dissertation a wide dynamic-range variable-gain transimpedance amplifier (TIA) is introduced. It adopts a regulated cascode (RGC) amplifier and an operational transconductance amplifier (OTA) as the feed forward gain element to control gain and improve the overload of the optical receiver. A fully-differential variable-gain TIA in a 0.35µm CMOS technology is realized. It provides a bit error rate (BER) less than 10-12 for an input current from 6µA-3mA at 3.3V power supply. For the transimpedance gain variation, from 0.1kΩ to 3kΩ, -3dB bandwidth is higher than 1.7GHz for a 0.6pF photodiode capacitance. The power dissipations for the highest and the lowest gains are 8.2mW and 24.9mW respectively. A new technique for designing uniform multistage amplifiers (MA) for high frequency applications is introduced. The proposed method uses the multi-peak bandwidth enhancement technique while it employs identical, simple and inductorless stages. It has several advantages, such as tunability of bandwidth and decreased sensitivity of amplifier stages, to process variations. While all stages of the proposed MA topology are identical, the gain-bandwidth product can be extended several times. Two six-stage amplifiers in a TSMC 0.35µm CMOS process were designed using the proposed topology. Measurements show that the gain can be varied for the first one between 16dB and 44dB within the 0.7-3.2GHz bandwidth and for the second one between 13dB and 44dB within a 1.9-3.7GHz bandwidth with less than 5.2nV/√Hz noise. Although the second amplifier has a higher gain bandwidth product, it consumes more power and occupies a wider area. A technique for capacitance multiplication is utilized to design a tunable loop filter. Current and voltage mode techniques are combined to increase the multiplication factor (M). At a high input dynamic range, M is adjustable and the capacitance multiplier performs linearly at high frequencies. Drain-source voltages of paired transistors are equalized to improve matching in the current mirrors. Measurement of a prototype loop filter IC in a 0.5µm CMOS technology shows 50µA current consumption for M=50. Where 80pF capacitance is employed, the capacitance multiplier realizes an effective capacitance varying from 1.22nF up to 8.5nF.