ABSTRACT

Time-Mode Analog Circuit Design for Nanometric Technologies

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Rapid scaling in technology has introduced new challenges in the realm of traditional analog design. Scaling of supply voltage directly impacts the available voltage-dynamic-range. On the other hand, nanometric technologies with fT in the hundreds of GHz range open opportunities for time-resolution-based signal processing. With reduced available voltage-dynamic-range and improved timing resolution, it is more convenient to devise analog circuits whose performance depends on edge-timing precision rather than voltage levels. Thus, instead of representing the data/information in the voltage-mode, as a difference between two node voltages, it should be represented in time-mode as a time-difference between two rising and/or falling edges. This dissertation addresses the feasibility of employing time-mode analog circuit design in different applications. Specifically: 1) Time-mode-based quanitzer and feedback DAC of SigmaDelta ADC. 2) Time-mode-based low-THD 10MHz oscillator, 3) A Spur-Frequency Boosting PLL with -74dBc Reference-Spur Rejection in 90nm Digital CMOS. In the first project, a new architectural solution is proposed to replace the DAC and the quantizer by a Time-to-Digital converter. The architecture has been fabricated in 65nm and shows that this technology node is capable of achieving a time-matching of 800fs which has never been reported. In addition, a competitive figure-of-merit is achieved. In the low-THD oscillator, I proposed a new architectural solution for synthesizing a highly-linear sinusoidal signal using a novel harmonic rejection approach. The chip is fabricated in 130nm technology and shows an outstanding performance compared to the state of the art. The designed consumes 80% less power; consumes less area; provides much higher amplitude while being composed of purely digital circuits and passive elements. Last but not least, the spur-frequency boosting PLL employs a novel technique that eliminates the reference spurs. Instead of adding additional filtering at the reference frequency, the spur frequency is boosted to higher frequency which is, naturally, has higher filtering effects. The prototype is fabricated in 90nm digital CMOS and proved to provide the lowest normalized reference spurs ever reported.