ABSTRACT

IF Subsampling Digital Radio Receiver. (May 2001)

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Portable wireless personal communication devices such as cellular phones, pagers, and wireless modems are increasingly becoming part of the daily life of millions. The advances in integrated circuit technology, digital communication methods, and digital signal processing are making them easier to use and packed with user friendly features. These devices must provide high data rate, and low power consumption for longer lasting battery life. The cost and size of such devices are also critical for their success in the consumer market.

In this dissertation, an implementation of a wireless receiver that utilizes the subsampling theorem is introduced. The main advantage of this receiver is the reduction of the number of components in the receiver, specially the components that usually cause degradation of the noise figure and consume more power, such as the second analog mixer in the heterodyne receiver. It also uses a single analog to digital converter instead of two in the case of any I-Q modulation and generates those I-Q paths all in the digital domain. Thus it eliminates any phase distortion caused by the analog I-Q path mismatch.

2G GSM standard was chosen as a case study to show the capability of this receiver to satisfy real specifications. The system design for this receiver is analyzed in details and explanation of the methodologies used to calculate the specifications for each block is discussed. System design simulation used to verify the specifications will be introduced and explained.

The circuit design of the Variable Gain Amplifier (VGA), which is considered a key block in the IF receiver chain, will be discussed in details. Different tradeoffs and the circuit techniques used to satisfy different specifications will be also discussed. Finally, the measurement results for this VGA as well as the whole receiver will be presented. This VGA operates at an IF frequency of 246MHz, and provides a digitally controlled 60dB-gain range in 2dB steps (with 0.3dB accuracy). Its noise figure is 8.7dB at maximum gain, and the OIP3 is –1dBm. The VGA consumes 9mA at 3V. It was fabricated in TSMC's 0.35μm CMOS process, occupying 0.64mm^2. The outstanding performance of this VGA puts it as a strong candidate for 3G applications as well.