Ph.D. Dissertation Abstract

Development of Robust Analog and Mixed-Signal Circuits in the Presence of Process-Voltage-Temperature Variations

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Continued improvements of transceiver systems-on-a-chip play a key role in the advancement of mobile telecommunication products as well as wireless systems in biomedical and remote sensing applications. This dissertation addresses the problems of escalating CMOS process variability and system complexity that diminish the reliability and testability of integrated systems, especially relating to the analog and mixed-signal blocks. The proposed design techniques and circuit-level attributes are aligned with current built-in testing and self-calibration trends for integrated transceivers. In this work, the main focus is on enhancing the performances of analog and mixed-signal blocks with digitally adjustable elements as well as with automatic analog tuning circuits, which are experimentally applied to conventional blocks in the receiver path in order to demonstrate the concepts.

The use of digitally controllable elements to compensate for variations is exemplified with two circuits. First, a distortion cancellation method for baseband operational transconductance amplifiers is proposed that enables a third-order intermodulation (IM3) improvement of up to 22dB. Fabricated in a 0.13μm CMOS process with 1.2V supply, a transconductance-capacitor lowpass filter with the linearized amplifiers has a measured IM3 below -70dB (with 0.2V peak-to-peak input signal) and 54.5dB dynamic range over its 195MHz bandwidth. The second circuit is a 3-bit two-step quantizer with adjustable reference levels, which was designed and fabricated in 0.18μm CMOS technology as part of a continuous-time ΣΔ analog-to-digital converter system. With 5mV resolution at a 400MHz sampling frequency, the quantizer's static power dissipation is 24mW and its die area is $0.4mm^2$.

An alternative to electrical power detectors is introduced by outlining a strategy for built-in testing of analog circuits with on-chip temperature sensors. Comparisons of an amplifier's measurement results at 1GHz with the measured DC voltage output of an on-chip temperature sensor show that the amplifier's power dissipation can be monitored and its 1-dB compression point can be estimated with less than 1dB error. The sensor has a tunable sensitivity up to 200mV/mW, a power detection range measured up to 16mW, and it occupies a die area of $0.012mm^2$ in standard 0.18μm CMOS technology.

Finally, an analog calibration technique is discussed to lessen the mismatch between transistors in the differential high-frequency signal path of analog CMOS circuits. The proposed methodology involves auxiliary transistors that sense the existing mismatch as part of a feedback loop for error minimization. It was assessed by performing statistical Monte Carlo simulations of a differential amplifier and a double-balanced mixer designed in CMOS technologies.