ABSTRACT

Low Power Filtering Techniques for Wideband and Wireless Applications

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This dissertation presents design and implementation of continuous time analog filters for two specific applications: wideband analog systems such as disk drive channel and low-power wireless applications. Specific focus has been techniques that reduce the power requirements of the overall system either through improvement in architecture or efficiency of the analog building blocks. The first problem that this dissertation addresses is the implementation of wideband filters with high equalization gain. An efficient architecture that realizes equalization zeros by combining available transfer functions associated with a biquadratic cell is proposed. A 330MHz, 5th order Gm-C lowpass Butterworth filter with 24dB boost is designed using the proposed architecture. The prototype fabricated in standard 0.35um CMOS process shows -41dB of IM3 for 250mV peak to peak swing with 8.6mW/pole of power dissipation. Also, an LC prototype implemented using similar architecture is discussed in brief. It is shown that, for practical range of frequency and SNR, LC based design is more power efficient than a Gm-C one, though at the cost of much larger area. Secondly, a complementary current mirror based building block is proposed, which pushes the limits imposed by conventional transconductors on the powerefficiency of Gm-C filters. Signal processing through complementary devices provides good linearity and Gm/Id efficiency and is shown to improve power efficiency by nearly 7 times. A current-mode 4th order Butterworth filter is designed, in 0.13um UMC technology, using the proposed building. It provides 54.2dB IM3 and 55dB SNR in 1.3GHz bandwidth while consuming as low as 24mW of power. All CMOS filter realization occupies a relatively small area and is well suited for integration in deep submicron technologies. Thirdly, a 20MHz, 68dB dynamic range active RC filter is presented. This filter is designed for a ten bit continuous time sigma delta ADC architecture developed specifically for fine-line CMOS technologies. Inverter based amplification and a common mode feedback for such amplifiers are discussed. The filter consumes 5mW of power and occupies an area of 0.07 mm2.