ABSTRACT

Low Voltage High Speed Switched Capacitor Circuit Design. (December, 2001) Lei Wang, B.S., Zhejiang University, China; M.S., Qinghua University, China Chair of Advisory Committee: Dr. S. H. K. Embabi

New methods were studied for the purpose of designing low voltage and high speed switched capacitor (SC) circuits without using the on-chip voltage bootstrapper. Auto-zeroed integrator (AZI) was proposed as the fundamental building block of low voltage SC systems. The AZI has no signal dependent switches, so it can work at the low voltage with a high operating speed. Also, the AZI is not sensitive to charge injection and non-linear resistance related distortions. The low voltage two-stage fully differential opamp built for the AZI has a dynamic common-mode feedback circuit without signal dependent switches. Three testing circuits using the AZI were implemented in the 1.2µm CMOS process at the 1.5V power supply voltage.

The first testing circuit is a second order fully differential SC bandpass filter working at 5.0MHz sampling rate. The central frequency of the filter is at 833KHz and the Q factor is 8. The second testing circuit is a fourth order fully differential SC bandpass delta-sigma modulator with the sampling rate of 5.0MHz too. It has a narrowband of 25KHz centered at the intermediate frequency (IF) of 1.25MHz. The tested results demonstrated a 60dB signal-to-noise-and-distortion-ratio (SNR) and a – 78dBc third order inter-modulation (IM3).

The third circuit is a 2-path fully differential fourth order bandpass delta-sigma modulator. It has an effective sampling rate of 10MHz double of the clock rate of 5.0MZ. The signal narrowband of the 2-path modulator is then located at 2.5MHz. The tested results are: 65 dB SNDR, -75dBc IM3, and a -35dBc spurious image of the desired signal.

As a supporting and extending research of SC circuits, a new architecture of the SC differentiator having less sensitivity to mismatch and lower thermal noise was also mentioned. A 2-path fourth order SC delta-sigma at the 3.0V supply voltage and 60MHz sampling rate was designed and implemented in 0.35µm CMOS process. The measured maximal SNR is 76dB for the 0.25V peak differential sine wave input.