Design of a 2.4-GHz CMOS Monolithic Fractional-N Frequency Synthesizer

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ABSTRACT :
The wireless communication technology and market have been growing rapidly since a decade ago. The high demand market is a driving need for higher integration in the wireless transceivers. The trend is to achieve low-cost, small form factor and low power consumption. With the ever-reducing feature size, it is becoming feasible to integrate the RF front-end together with the baseband in the low-cost CMOS technology. The frequency synthesizer is a key building block in the RF front-end of the transceivers. It is used as a local oscillator for frequency translation and channel selection. The design of a fully integrated 2.4-GHz low-power frequency synthesizer in 0.35um CMOS is a challenging task mainly due to the high-speed prescaler, and the on-chip integration of the loop filter.

In this dissertation, a brief review of the existing analysis and design techniques of PLL and frequency synthesizers is provided. Design techniques of a2.4-GHz monolithic SD fractional-N frequency synthesizer are investigated. Novel techniques are proposed to tackle the speed and integration bottlenecks of a high-frequency PLL. A low-power and inherently glitch-free phase-switching prescaler and an on-chip loop filter with capacitance multiplier are developed. Compared with the existing and popular dual-path topology, the proposed loop filter reduces circuit complexity and its power consumption and noise are negligible. Furthermore, a third-order three-level digital SD modulator topology is employed to reduce the phase noise generated by the modulator. Suitable PFD and charge-pump designs are employed to reduce their nonlinearity effects and thus minimize the folding of the SD modulator-shaped phase noise. A prototype of the fractional-N synthesizer and some standalone building blocks are designed and fabricated in TSMC 0.35um CMOS through MOSIS. The prototype frequency synthesizer and standalone prescaler and loop filter are characterized. The feasibility and practicality of the proposed prescaler and loop filter are experimentally verified

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