ABSTRACT

Analog and Mixed Signal Design towards a Miniaturized Sleep Apnea Monitoring Device
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Sleep apnea is a sleep-induced breathing disorder with symptoms of momentary and often repetitive cessations in breathing rhythm or sustained reductions in breathing amplitude. The phenomenon is known to occur with varying degrees of severity in literally millions of people around the world and cause a range of chronicle health issues. In spite of its high prevalence and serious consequences, nearly 80% of people with sleep apnea condition remain undiagnosed. The current standard diagnosis technique, termed polysomnography or PSG, requires the patient to schedule and undergo a complex full-night sleep study in a specially-equipped sleep lab. Due to both high cost and substantial inconvenience, millions of apnea patients are still undiagnosed and thus untreated. This research work aims at a simple, reliable, and miniaturized solution for in-home sleep apnea diagnosis purposes. The proposed solution bears high-level integration and minimal interference with sleeping patients, allowing them to monitor their apnea conditions at the comfort of their homes. Based on a MEMS sensor and an effective apnea detection algorithm, a low-cost single-channel apnea screening solution is proposed. A custom designed IC chip implements the apnea detection algorithm using time-domain signal processing techniques. The chip performs autonomous apnea detection and scoring based on the patient's airflow signals detected by the MEMS sensor. Variable sensitivity is enabled to accommodate different breathing signal amplitudes. The IC chip was fabricated in standard 0.5-μm CMOS technology. A prototype device was designed and assembled including a MEMS sensor, the apnea detection IC chip, a PSoC platform, and wireless transceiver for data transmission. The prototype device demonstrates a valuable screening solution with great potential to reach the broader public with undiagnosed apnea conditions. In a battery-operated miniaturized medical device, an energy-efficient analog-to-digital converter is an integral part linking the analog world of biomedical signals and the digital domain with powerful signal processing capabilities. This dissertation includes the detailed design of a successive approximation register (SAR) ADC for ultra-low power applications. The ADC adopts an asynchronous 2b/step scheme that halves both conversion time and DAC/digital circuit's switching activities to reduce static and dynamic energy consumption. A low-power sleep mode is engaged at the end of all conversion steps during each clock period. The technical contributions of this ADC design include an innovative 2b/step reference scheme based on a hybrid R-2R/C-3C DAC, an interpolation-assisted time-domain 2b comparison scheme, and a TDC with dual-edge-comparison mechanism. The prototype ADC was fabricated in 0.18μm CMOS process with an active area of 0.103 mm^(2), and achieves an ENoB of 9.2 bits and an FoM of 6.7 fJ/conversion-step at 100-kS/s.