ABSTRACT

Design of CMOS integrated frequency synthesizers for ultra-wideband wireless communications systems

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Ultra-wide band (UWB) system is a breakthrough in wireless communication, as it provides data rate one order higher than existing ones. This dissertation focuses on the design of CMOS integrated frequency synthesizer and its building blocks used in UWB system. A mixer based frequency synthesizer architecture is proposed to satisfy the agile frequency hopping requirement, which is no more than 9.5 ns, three orders faster than conventional phase locked loop (PLL) based synthesizers. Harmonic cancelation technique is extended and applied to suppress the undesired harmonic mixing components. Simulation shows that sidebands at 2.4 GHz and 5 GHz are below 36 dBc from carrier. The frequency synthesizer contains a novel quadrature VCO based on the capacitive source degeneration structure. The QVCO tackles the jeopardous ambiguity of the oscillation frequency in conventional QVCOs. Measurement shows that the 5 GHz CSD QVCO in 0.18 μm CMOS technology draws 5.2 mA current from a 1.2 V power supply. Its phase noise is 120 dBc at 3 MHz offset. Compared with existing phase shift LC QVCOs, the proposed CSD¬QVCO presents better phase noise and power efficiency. Finally, a novel injection locking frequency divider (ILFD) is presented. Implemented with three stages in 0.18 μm CMOS technology, the ILFD draws 3 mA current from a 1.8 V power supply. It achieves multiple large division ratios as 6, 12, and 18 with all locking ranges greater than 1.7 GHz and injection frequency up to 11 GHz. Compared with other published ILFDs, the proposed ILFD achieves the largest division ratio with satisfactory locking range.