

Fully-Integrated Building Blocks for Wireless Communication Transceiver Front-Ends on Silicon

May 2002

Fikret DULGER

Abstract

Three main contributions presented in this work are:

- i) Design techniques in a CMOS LC symmetric Voltage-Controlled Oscillator (VCO) with spiral inductors and bulk-tuned PMOS capacitors. Source-degeneration resistors used to linearize the negative conductance generator provide additional design degrees of freedom, trading the close-in phase noise with the phase noise at large offsets. Measured frequency tuning range around 2.15GHz is 3.5 % due to the limitation of the well resistance of the bulk-tuned capacitors. Phase noise of the VCO was calculated based on the Linear Time-Variant Impulse Sensitivity Function (ISF) theory and compared to the measured results. The VCO implemented in a 0.5 μm CMOS technology sinks 4mA from a 3V supply.
- ii) Design considerations in a dual-modulus divide by 32/33 prescaler with a 0.6 μm BiCMOS process. The phase noise contribution of the integrated bandgap bias network is demonstrated through simulations. The trade-off between the power consumption and the phase noise is pointed out and some guidelines are provided for improvement. Measurements confirm the functionality of the prescaler with a 2.5V supply drawing around 2.3mA at 2.35GHz. Input sensitivity is between -24dBm and 12dBm.
- iii) Design trade-offs of a fully-integrated Q-enhancement LC Bandpass Biquad programmable in peak gain, Q and f_0 . The circuit implemented in a 0.35 μm standard CMOS technology operates at 2.1GHz consuming 5mW at 1.3V supply. It uses a resonator built with spiral inductors and inversion-mode PMOS capacitors that provide frequency tuning. The Q tuning is through an adjustable negative-conductance generator. Noise and nonlinearity analyses presented demonstrate the design trade-offs involved. Measured frequency tuning range around 2.1GHz is 13%. The filter has a 1dB compression point dynamic range of 35dB and a spurious-free dynamic range of 31dB with a Q of 40 at 2.19GHz. The silicon area is 0.1mm². The filter introduced uses the lowest power supply voltage and the lowest power consumption per pole and occupies at least four times less silicon area per pole among the similar filters reported in the literature.