# ABSTRACT

Multi-Loop-Ring-Oscillator Design and Analysis for Sub-Micron CMOS

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Ring oscillators provide a central role in timing circuits for today?s mobile devices and desktop computers. Increased integration in these devices exacerbates switching noise on the supply, necessitating improved supply resilience. Furthermore, reduced voltage headroom in submicron technologies limits the number of stacked transistors available in a delay cell. Hence, conventional single-loop oscillators offer relatively few design options to achieve desired specifications, such as supply rejection. Existing state-of-the-art supply-rejection-enhancement methods include actively regulating the supply with an LDO, employing a fully differential or current-starved delay cell, using a hi-Z voltage-to-current converter, or compensating/calibrating the delay cell. Multiloop ring oscillators (MROs) offer an additional solution because by employing a more complex ring-connection structure and associated delay cell, the designer obtains an additional degree of freedom to meet the desired specifications. Designing these more complex multiloop structures to start reliably and achieve the desired performance requires a systematic analysis procedure, which we attack on two fronts: (1) a generalized delay-cell viewpoint of the MRO structure to assist in both analysis and circuit layout, and (2) a survey of phase-noise analysis to provide a bank of methods to analyze MRO phase noise. We distill the salient phase-noise-analysis concepts/key equations previously developed to facilitate MRO and other non-conventional oscillator analysis. Furthermore, our proposed analysis framework demonstrates that all these methods boil down to obtaining three things: (1) noise modulation function (NMF), (2) noise transfer function (NTF), and (3) current-controlled-oscillator gain (KICO). As a case study, we detail the design, analysis, and measurement of a proposed multiloop ring oscillator structure that provides improved power-supply isolation (more than 20dB increase in supply rejection over a conventional-oscillator control case fabricated on the same test chip). Applying our general multi-loop-oscillator framework to this proposed MRO circuit leads both to design-oriented expressions for the oscillation frequency and supply rejection as well as to an efficient layout technique facilitating cross-coupling for improved quadrature accuracy and systematic, substantially simplified layout effort.