ABSTRACT

Linearity and Noise Improvement Techniques Employing Low Power in Analog and RF Circuits and Systems

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The implementation of highly integrated multi-bands and multi-standards reconfigurable radio transceivers is one of the great challenges in the area of integrated circuit technology today. In addition the rapid market growth and high quality demands that require cheaper and smaller solutions, the technical requirements for the transceiver function of a typical wireless device are considerably multi-dimensional. The major key performance metrics facing RFIC designers are power dissipation, speed, noise, linearity, gain, and efficiency. Beside the difficulty of the circuit design due to the trade-offs and correlations that exist between these parameters, the situation becomes more and more challenging when dealing with multi-standard radio systems on a single chip and applications with different requirements on the radio software and hardware aiming at highly flexible dynamic spectrum access. In this dissertation, different solutions are proposed to improve the linearity, reduce the noise and power consumption in analog and RF circuits and systems.

A system level design digital approach is proposed to compensate the harmonic distortion components produced by transmitter circuits' nonlinearities. The approach relies on polyphase multipath scheme uses digital baseband phase rotation pre-distortion aiming at increasing harmonic cancellation and power consumption reduction over other reported techniques.

New low power design techniques to enhance the noise and linearity of the receiver front-end LNA are also presented. The two proposed LNAs are fully differential and have a common-gate capacitive cross-coupled topology. The proposed LNAs avoids the use of bulky inductors that leads to area and cost saving. Prototypes are implemented in IBM 90 nm CMOS technology for the two LNAs. The first LNA covers the frequency range of 100 MHz to 1.77 GHz consuming 2.8 mW from a 2 V supply. Measurements show a gain of 23 dB with a 3-dB bandwidth of 1.76 GHz. The minimum NF is 1.85 dB while the input return loss is greater than 10 dB across the entire band. The second LNA covers the frequency range of 100 MHz to 1.6 GHz. A 6 dBm third-order input intercept point, IIP_3, is measured at the maximum gain frequency. The core consumes low power of 1.55 mW using a 1.8 V supply. The measured voltage gain is 15.5 dB with a 3-dB bandwidth of 1.6 GHz. The LNA has a minimum NF of 3 dB across the whole band while achieving an input return loss greater than 12 dB.

Finally, A CMOS single supply operational transconductance amplifier (OTA) is reported. It has high power supply rejection capabilities over the entire gain bandwidth (GBW). The OTA is fabricated on the AMI 0.5 um

CMOS process. Measurements show power supply rejection ratio (PSRR) of 120 dB till 10 KHz. At 10 MHz, PSRR is 40 dB. The high performance PSRR is achieved using a high impedance current source and two noise reduction techniques. The OTA offers a very low current consumption of 25 uA from a 3.3 V supply