Abstract
Analog integrated circuit design techniques for high-speed signal processing in communications systems
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This work presents design techniques for the implementation of high-speed analog integrated circuits for wireless and wireline communications systems. Limitations commonly found in high-speed switched-capacitor (SC) circuits used for intermediate frequency (IF) filters in wireless receivers are explored. A model to analyze the aliasing effects due to periodical non-uniform individual sampling, a technique used in high-Q high-speed SC filters, is presented along with practical expressions that estimate the power of the generated alias components. The results are verified through circuit simulation of a 10.7MHz bandpass SC filter in TSMC 0.35μm CMOS technology. Implications on the use of this technique on the design of IF filters are discussed. To improve the speed at which SC networks can operate, a continuous-time common-mode feedback (CMFB) with reduced loading capacitance is proposed. This increases the achievable gain-bandwidth product (GBW) of fully-differential amplifiers. The performance of the CMFB is demonstrated in the implementation of a second-order 10.7MHz bandpass SC filter and compared with that of an identical filter using the conventional switched-capacitor CMFB (SC-CMFB). The filter using the continuous-time CMFB reduces the error due to finite GBW and slew rate to less than 1% for clock frequencies up to 72MHz while providing a dynamic range of 59dB and a PSRR- > 22dB. The design of high-speed transversal equalizers for wireline transceivers requires the implementation of broadband delay lines. A delay line based on a third-order linear-phase filter is presented for the implementation of a fractionally-spaced 1Gb/s transversal equalizer. Two topologies for a broadband summing node which enable the placement of the parasitic poles at the output of the transversal equalizer beyond 650MHz are presented. Using these cells, a 5-tap 1Gb/s equalizer was implemented in TSMC 0.35μm CMOS technology. The results show a programmable frequency response able to compensate up to 25dB loss at 500MHz. The eye-pattern diagrams at 1Gb/s demonstrate the equalization of 15 meters and 23 meters of CAT5e twistedpair cable, with a vertical eye-opening improvement from 0% (before the equalizer) to 58% (after the equalizer) in the second case. The equalizer consumes 96mW and an area of 630μm x 490μm.