ABSTRACT

Radio Frequency Circuits for Wireless Receiver Front-ends. (August 2004) Chunyu Xin, B.S., Nankai University, China; M.S., Nankai University, China

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

The beginning of the 21st century sees great development and demands on wireless communication technologies. Wireless technologies, either based on a cable replacement or on a networked environment, penetrate our daily life more rapidly than ever. Low operational power, low cost, small form factor, and function diversity are the crucial requirements for a successful wireless product. The receiver's front-end circuits play an important role in faithfully recovering the information transmitted through the wireless channel.

Bluetooth is a short-range cable replacement wireless technology. A Bluetooth receiver architecture was proposed and designed using a pure CMOS process. The front-end of the receiver consists of a low noise amplifier (LNA) and mixer. The intermediate frequency was chosen to be 2MHz to save battery power and alleviate the low frequency noise problem. A conventional LNA architecture was used for reliability. The mixer is a modified Gilbert-cell using the current bleeding technique to further reduce the low frequency noise. The front-end draws 10 mA current from a 3 V power supply, has a 8.5 dB noise figure, and a voltage gain of 25 dB and -9 dBm IIP3.

A front-end for dual-mode receiver is also designed to explore the capability of a multi-standard application. The two standards are IEEE 802.11b and Bluetooth. They work together making the wireless experience more exciting. The front-end is designed using BiCMOS technology and incorporating a direct conversion receiver architecture. A number of circuit techniques are used in the front-end design to achieve optimal results. It consumes 13.6 mA from a 2.5 V power supply with a 5.5 dB noise figure, 33 dB voltage gain and -13 dBm IIP3.

Besides the system level contributions, intensive studies were carried out on the development of quality LNA circuits. Based on the multi-gated LNA structure, a CMOS LNA structure using bipolar transistors to provide linearization is proposed. This LNA configuration can achieve comparable linearity to its CMOS multi-gated counterpart and work at a higher frequency with less power consumption. A LNA using an on-chip transformer source degeneration is proposed to realize input impedance matching. The possibility of a dual-band cellular application is studied. Finally, a study on ultra-wide band (UWB) LNA implementation is performed to explore the possibility and capability of CMOS technology on the latest UWB standard for multi-media applications.