# ABSTRACT

Calibrated Continuous-Time Sigma-Delta Modulators

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To provide more information mobility, many wireless communication systems such as WCDMA and EDGE in phone systems, bluetooth and WIMAX in communication networks have been recently developed. Recent efforts have been made to build the allin- one next generation device which integrates a large number of wireless services into a single receiving path in order to raise the competitiveness of the device. Among all the receiver architectures, the high-IF receiver presents several unique properties for the next generation receiver by digitalizing the signal at the intermediate frequency around a few hundred MHz. In this architecture, the modulation/demodulation schemes, protocols, equalization, etc., are all determined in a software platform that runs in the digital signal processor (DSP) or FPGA. The specifications for most of front-end building blocks are relaxed, except the analog-to-digital converter (ADC). The requirements of large bandwidth, high operational frequency and high resolution make the design of the ADC very challenging. Solving the bottleneck associated with the high-IF receiver architecture is a major focus of many ongoing research efforts. In this work, a 6th-order bandpass continuous time sigma-delta ADC with measured 68.4dB SNDR at 10MHz bandwidth to accommodate video applications is proposed. Tuned at 200 MHz, the fs/4 architecture employs an 800 MHz clock frequency. By making use of a unique software-based calibration scheme together with the tuning properties of the bandpass filters developed under the umbrella of this project, the ADC performance is optimized automatically to fulfill all requirements for the high-IF architecture. In a separate project, other critical design issues for continuous-time sigma-delta ADCs are addressed, especially the issues related to unit current source mismatches in multi-level DACs as well as excess loop delays that may cause loop instability. The reported solutions are revisited to find more efficient architectures. The aforementioned techniques are used for the design of a 25MHz bandwidth lowpass continuous-time sigma-delta modulator with time-domain two-step 3-bit quantizer and DAC for WiMAX applications. The prototype is designed by employing a level-to-pulse-width modulation (PWM) converter followed by a single-level DAC in the feedback path to translate the typical digital codes into PWM signals with the proposed pulse arrangement. Therefore, the non-linearity issue from current source mismatch in multi-level DACs is prevented. The jitter behavior and timing mismatch issue of the proposed time-based methods are fully analyzed. The measurement results of a chip prototype achieving 67.7dB peak SNDR and 78dB SFDR in 25MHz bandwidth properly demonstrate the design concepts and effectiveness of time-based quantization and feedback. Both continuous-time sigma-delta ADCs were fabricated

in mainstream CMOS 0.18um technologies, which are the most popular in today?s consumer electronics industry.