ABSTRACT

Design and Implementation of Frequency Synthesizers for 3-10 GHz Multiband OFDM UWB Communication. (December 2007)

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The allocation of frequency spectrum by the FCC for Ultra Wideband (UWB) communications in the 3.1-10.6 GHz has paved the path for very high data rate Gb/s wireless communications. Frequency synthesis in these communication systems involves great challenges such as high frequency and wideband operation in addition to stringent requirements on frequency hopping time and coexistence with other wireless standards. This research proposes frequency generation schemes for such radio systems and their integrated implementations in silicon based technologies. Special emphasis is placed on efficient frequency planning and other system level considerations for building compact and practical systems for carrier frequency generation in an integrated UWB radio.

This work proposes a frequency band plan for multiband OFDM based UWB radios in the 3.1-10.6 GHz range. Based on this frequency plan, two 11-band frequency synthesizers are designed, implemented and tested making them one of the first frequency synthesizers for UWB covering 78% of the licensed spectrum. The circuits are implemented in 0.25μm SiGe BiCMOS and the architectures are based on a single VCO

at a fixed frequency followed by an array of dividers, multiplexers and single sideband (SSB) mixers to generate the 11 required bands in quadrature with fast hopping in much less than 9.5 ns. One of the synthesizers is integrated and tested as part of a 3-10 GHz packaged receiver. It draws 80 mA current from a 2.5 V supply and occupies an area of 2.25 mm^2.

Finally, an architecture for a UWB synthesizer is proposed that is based on a single multiband quadrature VCO, a programmable integer divider with 50% duty cycle and a single sideband mixer. A frequency band plan is proposed that greatly relaxes the tuning range requirement of the multiband VCO and leads to a very digitally intensive architecture for wideband frequency synthesis suitable for implementation in deep submicron CMOS processes. A design in 130nm CMOS occupies less than 1 mm^2 while consuming 90 mW. This architecture provides an efficient solution in terms of area and power consumption with very low complexity.