Low-Power Low-Noise CMOS Analog and Mixed-Signal Design towards Epileptic Seizure Detection

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ABSTRACT

About 50 million people worldwide suffer from epilepsy and one third of them have seizures that are refractory to medication. In the past few decades, deep brain stimulation (DBS) has been explored by researchers and physicians as a promising way to control and treat epileptic seizures. To make the DBS therapy more efficient and effective, the feedback loop for titrating therapy is required. It means the implantable DBS devices should be smart enough to sense the brain signals and then adjust the stimulation parameters adaptively.

This research proposes a signal-sensing channel configurable to various neural applications, which is a vital part for a future closed-loop epileptic seizure stimulation system. This doctoral study has two main contributions, 1) a micropower low-noise neural front-end circuit, and 2) a low-power configurable neural recording system for both neural action-potential (AP) and fast-ripple (FR) signals.

The neural front end consists of a preamplifier followed by a bandpass filter (BPF). This design focuses on improving the noise-power efficiency of the preamplifier and the power/pole merit of the BPF at ultra-low power consumption. In measurement, the preamplifier exhibits

39.6-dB DC gain, 0.8 Hz to 5.2 kHz of bandwidth (BW), 5.86-μV_{rms} input-referred noise in AP mode, while showing 39.4-dB DC gain, 0.36 Hz to 1.3 kHz of BW, 3.07-μV_{rms} noise in FR mode. The preamplifier achieves noise efficiency factor (NEF) of 2.93 and 3.09 for AP and FR modes, respectively. The preamplifier power consumption is 2.4 μW from 2.8 V for both modes. The 6^{th}-order follow-the-leader feedback elliptic BPF passes FR signals and provides -110 dB/decade attenuation to out-of-band interferers. It consumes 2.1 μW from 2.8 V (or 0.35 μW/pole) and is one of the most power-efficient high-order active filters reported to date. The complete front-end circuit achieves a mid-band gain of 38.5 dB, a BW from 250 to 486 Hz, and a total input-referred noise of 2.48 μV_{rms} while consuming 4.5 μW from the 2.8 V power supply. The front-end NEF achieved is 7.6. The power efficiency of the complete front-end is 0.75 μW/pole. The chip is implemented in a standard 0.6-μm CMOS process with a die area of 0.45 mm^2.

The neural recording system incorporates the front-end circuit and a sigma-delta analog-to-digital converter (ADC). The ADC has scalable BW and power consumption for digitizing both AP and FR signals captured by the front end. Various design techniques are applied to the improvement of power and area efficiency for the ADC. At 77-dB dynamic range (DR), the ADC has a peak SNR and SNDR of 75.9 dB and 67 dB, respectively, while consuming 2.75-mW power in AP mode. It achieves 78-dB DR, 76.2-dB peak SNR, 73.2-dB peak SNDR, and 588-μW power consumption in FR mode. Both analog and digital power supply voltages are 2.8 V. The chip is fabricated in a standard 0.6-μm CMOS process. The die size is 11.25 mm^2.

The proposed circuits can be extended to a multi-channel system, with the ADC shared by all channels, as the sensing part of a future closed-loop DBS system for the treatment of intractable epilepsy.