

ABSTRACT

Analog-to-Digital Interface Design for Wireless Receivers (December 2004)

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As one of the major building blocks in a wireless receiver, the Analog-to-Digital Interface (ADI) provides link and transition between the analog Radio Frequency (RF) frontend and the baseband Digital Signal Processing (DSP) module. The rapid development of the radio technologies raises new design challenges for the receiver ADI implementation. Requirements, such as power consumption optimization, multi-standard compatibility, fast settling capability and wide signal bandwidth capacity, are often encountered in a low voltage ADI design environment. Previous research offers ADI design schemes that emphasize individual merit. A systematic ADI design methodology is, however, not sufficiently studied. In this work, the ADI design for two receiver systems are employed as research vehicles to provide solutions for different ADI design issues.

A zero-crossing demodulator ADI is designed in the 0.35 μ m CMOS technology for the Bluetooth receiver to provide fast settling. Architectural level modification improves the process variation and the Local Oscillation (LO) frequency offset immunity of the demodulator. A 16.2dB Signal-to-Noise Ratio (SNR) at 0.1% Bit Error Rate (BER) is achieved with less than 9mW power dissipation in the lab measurement. For ADI in the 802.11b/Bluetooth dual-mode-receiver, a configurable time-interleaved pipeline Analog-to-Digital-Converter (ADC) structure is adopted to provide the required

multi-standard compatibility. An online digital calibration scheme is also proposed to compensate process variation and mismatching. The prototype chip is fabricated in the 0.25 μ m BiCMOS technology. Experimentally, an SNR of 60dB and 64dB are obtained under the 802.11b and Bluetooth receiving modes, respectively. The power consumption of the ADI is 20.2mW under the receiving mode and 14.8mW under the Bluetooth mode.

In this dissertation, each step of the receiver ADI design procedure, from system level optimization to the transistor level implementation and lab measurement, is illustrated in detail. The observations are carefully studied to provide insight on receiver ADI design issues. The ADI design for the Ultra-Wide Band (UWB) receiver is also studied at system level. Potential ADI structure is proposed to satisfy the wide signal bandwidth and high speed requirements for future applications.