

Abstract

Design of RF/IF analog to digital converters for software radio communication receivers

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Bharath Kumar Thandri

Chair of Advisory Committee: Jose Silva-Martinez

Software radio architecture can support multiple standards by performing analog-to-digital (A/D) conversion of the radio frequency (RF) signals and running reconfigurable software programs on the backend digital signal processor (DSP). A slight variation of this architecture is the software defined radio architecture in which the A/D conversion is performed on intermediate frequency (IF) signals after a single down conversion. The first part of this research deals with the design and implementation of a fourth order continuous time bandpass sigma-delta (CT BP) C based on LC filters for direct RF digitization at 950 MHz with a clock frequency of 3.8 GHz. A new ADC architecture is proposed which uses only non-return to zero feedback digital to analog converter pulses to mitigate problems associated with clock jitter. The architecture also has full control over tuning of the coefficients of the noise transfer function for obtaining the best signal to noise ratio (SNR) performance. The operation of the architecture is examined in detail and extra design parameters are introduced to ensure robust operation of the ADC. Measurement results of the ADC, implemented in IBM 0.25 μm SiGe BiCMOS technology, show SNR of 63 dB and 59 dB in signal bandwidths of 200 kHz and 1 MHz, respectively, around 950 MHz while consuming 75 mW of power from ± 1.25 V supply. The second part of this research deals with the design of a fourth order CT BP ADC based on gm-C integrators with an automatic digital tuning scheme for IF digitization at 125 MHz and a clock frequency of 500 MHz. A linearized CMOS OTA architecture combines both cross coupling and source degeneration in order to obtain good IM3 performance. A system level digital tuning scheme is proposed to tune the ADC performance over process, voltage and temperature variations. The output bit stream of the ADC is captured using an external DSP, where a software tuning algorithm tunes the ADC parameters for best SNR performance. The IF ADC was designed in TSMC 0.35 μm CMOS technology and it consumes 152 mW of power from ± 1.65 V supply.