ABSTRACT

Design Methodology for Mixed-Signal AC BIST

and ADC Self-Calibration. (May 2002)

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The contributions on the work here presented involved two main parts: a) Design Methodology for Mixed-Signal AC BIST and b) An ADC Self-Calibration Implementation Scheme.

The first approach, called *Time-Domain Testing*, analyses the step response of a DUT (Device Under Test) in time-domain by measuring several rise and fall times. The system uses a self-calibrating ramp generator as an analog timer, which uses an analog discrete-time adaptive scheme. Four implementations are presented for different levels of accuracy and complexity. Measurement results show excellent accuracy and programmability (variable tuning range of 0.4V/ms to 2V/ms, or 4 selectable settings of 1.7, 6.8, 218 and 870V/ms). Slope error is only 0.6% and maximum INL error is ±15μV in post-layout simulations and ±175μV in measurement (limited by test setup accuracy). A complete time-domain test system is presented.

The second approach, called *Inverted Stimulus*, uses the inverse of the DUT's transfer function to pre-shape the input step signal before applying it to the DUT. This approach greatly simplifies the precision requirements on the circuits in the analysis block. Issues of bounded signals in the inverse transfer function are discussed, and results showing excellent fault coverage (10% variation on the cutoff frequency or steady-state value of a 4^{th} order Leapfrog filter) are presented.

The dissertation presents the design of a unified scheme for self-calibration and self-test of pipeline ADCs. Except for a self-calibrating on-chip ramp generator, the whole calibration process is performed in digital domain, therefore ensuring robustness, process independence and compatibility with external digital test equipment. Consistent improvements of more than 2 bits on the INL (Integral Non-Linearity) are obtained under noisy environment. The circuit includes an accurate built-in INL computation block.