ABSTRACT

Design of Frequency Synthesizers for Short RangeWireless Transceivers.

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The rapid growth of the market for short-range wireless devices, with standards such as Bluetooth and Wireless LAN (IEEE 802.11) being the most important, has created a need for highly integrated transceivers that target drastic power and area reduction while providing a high level of integration. The radio section of the devices designed to establish communications using these standards is the limiting factor for the power reduction efforts. A key building block in a transceiver is the frequency synthesizer, since it operates at the highest frequency of the system and consumes a very large portion of the total power in the radio. This dissertation presents the basic theory and a design methodology of frequency synthesizers targeted for short-range wireless applications. Three different examples of synthesizers are presented. First a frequency synthesizer integrated in a Bluetooth receiver fabricated in 0.35µm CMOS technology. The receiver uses a low-IF architecture to downconvert the incoming Bluetooth signal to 2MHz.

The second synthesizer is integrated within a dual-mode receiver capable of processing signals of the Bluetooth and Wireless LAN (IEEE 802.11b) standards. It is implemented in BiCMOS technology and operates the voltage controlled oscillator at

twice the required frequency to generate quadrature signals through a divide-by-two circuit. A phase switching prescaler is featured in the synthesizer. A large capacitance is integrated on-chip using a capacitance multiplier circuit that provides a drastic area reduction while adding a negligible phase noise contribution.

The third synthesizer is an extension of the second example. The operation range of the VCO is extended to cover a frequency band from 4.8GHz to 5.85GHz. By doing this, the synthesizer is capable of generating LO signals for Bluetooth and IEEE 802.11a, b and g standards. The quadrature output of the 5 – 6 GHz signal is generated through a first order RC – CR network with an automatic calibration loop. The loop uses a high frequency phase detector to measure the deviation from the 90° separation between the *I* and *Q* branches and implements an algorithm to minimize the phase errors between the *I* and *Q* branches and their differential counterparts.