ABSTRACT

Monolithic Implementation of Turbo Codes. (May 2002)

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Turbo codes were discovered in 1993; they consist of the parallel concatenation of recursive systematic convolutional coders separated by interleavers and use soft-input soft-output iterative decoders. Turbo codes have become a standard technique for channel coding due to their simplicity and performance.

One of the key aspects of turbo codes is that they use soft-input and soft-output values in the decoding stage. Thus no information is discarded until the algorithm has iteratively converged to a solution, at which time a hard decision is taken. The soft-input soft-output concept refers to infinite quantized or analog values in a natural form.

This research work proposes CMOS integrated circuit implementations of both the encoding and the decoding algorithms. In particular it explores an all-analog decoder implementation that will naturally exploit the continuous nature of the received signals.

The proposed analog decoder is based on the additive soft-input soft-output algorithm that can be naturally mapped into a multiple input floating gate transistors implementation. By taking advantage of the symmetric structure of the trellis generated

by convolutional codes, every node in the trellis can have a direct analog counterpart that will mathematically solve the decoding algorithm in the analog domain.

A normalization circuitry is included to restore the signal levels at each stage; this block results in a large area compared to the area used by the algorithm computing cells. The normalization procedure utilizes negative feedback techniques to automatically restore the amplitude and offset levels required.

In addition, a complete characterization and modeling methodology for multiple input floating gate transistors is presented. The multiple input floating gate devices used are based on a new structure that has an additional voltage input through an n-well. This input can be used for calibration, noise isolation or as an additional input.

Complete design-flows for both digital and analog integrated circuit designs are presented. Theoretical results are validated by the fabrication and testing of digital and analog integrated circuits in CMOS technology.