ABSTRACT

System-level design and RF Front-End Implementation for a 3-10GHz MultiBand-OFDM UltraWideBand Receiver and Built-In Testing Techniques for Analog and RF Integrated Circuits. (May 2006)

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This work consists of two main parts: a) Design of a 3-10GHz UltraWideBand (UWB) Receiver and b) Built-In Testing Techniques (BIT) for Analog and RF circuits.

The MultiBand OFDM (MB-OFDM) proposal for UWB communications has received significant attention for the implementation of very high data rate (up to 480Mb/s) wireless devices. I was honored to lead the efforts of a team of 4 graduate students in the development of an 11-band 3.4-10.3GHz direct conversion receiver for MB-OFDM UWB implemented in a 0.25mm BiCMOS process. I was responsible for the system-level design as well as the design of the LNA and down-conversion quadrature mixer. The packaged IC includes an RF front-end with interference rejection at 5.25GHz, a frequency synthesizer generating 11 carrier tones in quadrature with fast hopping, and a linear phase baseband section with 42dB of gain programmability. The receiver IC mounted on a FR-4 substrate provides a maximum gain of 67-78dB and NF of 5-10dB across all bands while consuming 114mA from a 2.5V supply.

Two BIT techniques for analog and RF circuits were developed. The goal is to reduce the test cost by reducing the use of analog instrumentation. An integrated frequency response characterization system with a digital interface is proposed to test the magnitude and phase responses at different nodes of an analog circuit. A complete prototype in CMOS 0.35mm technology employs only 0.3mm2 of area. Its operation is demonstrated by performing frequency response measurements in a range of 1 to 130MHz on 2 analog filters integrated on the same chip. A very compact CMOS RF RMS Detector and a methodology for its use in the built-in measurement of the gain and 1dB compression point of RF circuits are proposed to address the problem of on-chip testing at RF frequencies. The proposed device generates a DC voltage proportional to the RMS voltage amplitude of an RF signal. A design in CMOS 0.35mm technology presents and input capacitance <15fF and occupies and area of 0.03mm2. The application of the combined use of these two techniques in the fault detection and diagnosis of a wireless transceiver is discussed.