

## ABSTRACT

Bluetooth/WLAN Receiver Design Methodology and  
IC Implementations. (December 2003)

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Emerging technologies such as Bluetooth and 802.11b (Wi-Fi) have fuelled the growth of the short-range communication industry. Bluetooth, the leading WPAN (wireless personal area network) technology, was designed primarily for cable replacement applications. The first generation Bluetooth products are focused on providing low-cost radio connections among personal electronic devices. In the WLAN (wireless local area network) arena, Wi-Fi appears to be the superior product. Wi-Fi is designed for high speed internet access, with higher radio power and longer distances. Both technologies use the same 2.4GHz ISM band. The differences between Bluetooth and Wi-Fi standard features lead to a natural partitioning of applications. Nowadays, many electronics devices such as laptops and PDAs, support both Bluetooth and Wi-Fi standards to cover a wider range of applications. The cost of supporting both standards, however, is a major concern. Therefore, a dual-mode transceiver is essential to keep the size and cost of such system transceivers at a minimum.

A fully integrated low-IF Bluetooth receiver is designed and implemented in a low cost, main stream 0.35 $\mu$ m CMOS technology. The system includes the RF front end, frequency synthesizer and baseband blocks. It has -82dBm sensitivity and draws 65mA current. This project involved six Ph.D. students and I was in charge of the design of the channel selection complex filter.

In the Bluetooth transmitter, a frequency modulator with fine frequency steps is needed to generate the GFSK signal that has  $\pm 160$ kHz frequency deviation. A low power ROM-less direct digital frequency synthesizer (DDFS) is designed to implement the frequency modulation. The DDFS can be used for any frequency or phase modulation communication systems that require fast frequency switching with fine frequency steps. Another contribution is the implementation of a dual-mode 802.11b/Bluetooth receiver in

IBM 0.25 $\mu$ m BiCMOS process. Direct-conversion architecture was used for both standards to achieve maximum level of integration and block sharing. I was honored to lead the efforts of seven Ph.D. students in this project. I was responsible for system level design as well as the design of the variable gain amplifier. The receiver chip consumes 45.6/41.3mA and the sensitivity is -86/-91dBm.