NYQUIST-RATE SWITCHED-CAPACITOR

ANALOG-TO-DIGITAL CONVERTERS

The miniaturization and digitization of modern microelectronic systems have made Analog-to-Digital converters (ADC) key building components in many applications. Internet and entertainment technologies demand higher and higher performance from the hardware components in many communication and multimedia systems, but at the same time increased mobility demands less and less power consumption. Many applications, such as instrumentation, video, radar and communications, require very high accuracy and speed and with resolutions up to 16 bits and sampling rates in the 100s of MHz, pipelined ADCs are very suitable for such purposes. Resolutions above 10 bits often require very high power consumption and silicon area if no error correction technique is employed. Calibration relaxes the accuracy requirement of the individual building blocks of the ADC and enables power and area savings. Digital calibration is preferred over analog calibration due to higher robustness and accuracy. Furthermore, the microprocessors that process the digital information from the ADCs have constantly reduced cost and power consumption and improved performance due to technology scaling and innovative microprocessor architectures.

The work in this dissertation presents a novel digital background calibration technique for high-speed, high-resolution pipelined ADCs. The technique is implemented in a 14 bit, 100 MS/s pipelined ADC fabricated in Taiwan Semiconductor Manufacturing

Company (TSMC) 0.13µm Complementary Metal Oxide Semiconductor (CMOS) digital technology. The prototype ADC achieves better than 11.5 bits linearity at 100 MS/s and achieves a best-in-class figure of merit of 360fJ/conversion-step. The core ADC has a power consumption of 105 mW and occupies an active area of 1.25 mm^2.

The work in this dissertation also presents a low-power, 8-bit algorithmic ADC. This ADC reduces power consumption at system level by minimizing voltage reference generation and ADC input capacitance. This ADC is implemented in International Business Machines Corporation (IBM) 90nm digital CMOS technology and achieves around 7.5 bits linearity at 0.25 MS/s with a power consumption of 300 µW and an active area of 0.27 mm^2.