ABSTRACT

Design of a 125 MHz Tunable Continuous-time Bandpass Modulator
for Wireless IF Applications. (December 2004)
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Bandpass sigma-delta modulators combine oversampling and noise shaping to get very high resolution in a limited bandwidth. They are widely used in applications that require narrowband high-resolution conversion at high frequencies. In recent years interests have been seen in wireless system and software radio using sigma-delta modulators to digitize signals near the front end of radio receivers. Such applications necessitate clocking the modulators at a high frequency (MHz or above). Therefore a loop filter is required in continuous-time circuits (e.g., using transconductors and integrators) rather than discrete-time circuits (e.g., using switched capacitors) where the maximum clocking rate is limited by the bandwidth of Opamp, switch's speed and settling-time of the circuitry.

In this work, the design of a CMOS fourth-order bandpass sigma-delta modulator clocking at 500 MHz for direct conversion of narrowband signals at 125 MHz is presented. A new calibration scheme is proposed for the best signal-to-noise-distortion-ratio (SNDR) of the modulator. The continuous-time loop filter is based on Gm-C resonators. A novel transconductance amplifier has been developed with high linearity at high frequency. Q-factor of filter is enhanced by tunable negative impedance which cancels the finite output impendence of OTA. The fourth-order modulator is implemented using 0.35 μm triple-metal standard analog CMOS technology. Postlayout simulation in CADENCE demonstrates that the modulator achieves a SNDR of 50 dB (~8 bit) performance over a 1 MHz bandwidth. The modulator's power consumption is 302 mW from supply power of ± 1.65V.