ABSTRACT

DESIGN OF THE TRANSCONDUCTANCE AMPLIFIER FOR FREQUENCY DOMAIN SAMPLING RECEIVER

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In this work, the circuit implementation of the front-end for Frequency Domain (FD) Sampling Receiver is presented. Shooting for two different applications, two transconductance amplifiers are designed. A high linear transconductance amplifier with 25 dBm IIP3 is proposed to form the high resolution and high sampling rate FD receiver. The whole system achieves an overall sampling rate of 2 Gs/s and resolution of 10 bits. Another low noise transconductance amplifier exploiting noise cancelling is designed to build up the FD wireless communication receiver, which is an excellent candidate for Software Define Radio (SDR) and Cognitve Radio (CR). The proposed noise cancelling scheme can suppress both thermal noise and flicker noise at the frontend. The system Noise Figure (NF) is improved by 3.28 dB. The two transconductance amplifiers are simulated and fabricated with TI 45nm CMOS technology.