

# ABSTRACT

System Design of a Wide Bandwidth Continuous-Time Sigma-Delta Modulator

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Sigma-delta analog-to-digital converters are gaining in popularity in recent times because of their ability to trade-off resolutions in the time and voltage domains. In particular, continuous-time modulators are finding more acceptance at higher bandwidths due to the additional advantages they provide, such as better power efficiency and inherent anti-aliasing filtering, compared to their discrete-time counterparts. This thesis work presents the system level design of a continuous-time low-pass sigma-delta modulator targeting 11 bits of resolution over 100MHz signal bandwidth. The design considerations and tradeoffs involved at the system level are presented. The individual building blocks in the modulators are modeled with non-idealities and specifications for the various blocks are obtained in detail. Simulation results obtained from behavioral models of the system in MATLAB and Cadence environment show that a signal-to-noise-and-distortion-ratio (SNDR) of 69.6dB is achieved. A loop filter composed of passive LC sections is utilized in place of integrators or resonators used in traditional modulator implementations. Gain in the forward signal path is realized using active circuits based on simple transconductance stages. A novel method to compensate for excess delay in the loop without using an extra summing amplifier is proposed.