

ABSTRACT

Filter Design Considerations for High Performance Continuous-Time Low-Pass Sigma-Delta ADC

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Continuous-time filters are critical components in the implementation of large bandwidth, high frequency, and high resolution continuous-time (CT) sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADCs). The loop filter defines the noise-transfer function (NTF) and hence the quantization noise-shaping behavior of the $\Sigma\Delta$ modulator, and becomes the most critical performance determining part in $\Sigma\Delta$ ADC. This thesis work presents the design considerations for the loop filter in low-pass CT $\Sigma\Delta$ ADC with 12-bits resolution in 25MHz bandwidth and low power consumption using 0.18 μm CMOS technology. Continuous-time filters are more suitable than discrete-time filters due to relaxed amplifier bandwidth requirements for high frequency $\Sigma\Delta$ ADCs. A fifth-order low-pass filter with cut-off frequency of 25 MHz was designed to meet the dynamic range requirement of the ADC. An active RC topology was chosen for the implementation of the loop filter, which can provide high dynamic range required by the $\Sigma\Delta$ ADC. The design of a summing amplifier and a novel method for adjusting the group delay in the fast path provided by a secondary feedback DAC of the $\Sigma\Delta$ ADC are presented in detail. The ADC was fabricated using Jazz 0.18 μm CMOS technology. The implementation issues of OTAs with high-linearity and low-noise performance suitable for the broadband ADC applications are also analyzed in this work. Important design equations pertaining to the linearity and noise performance of the Gm-C biquad filters are presented. A Gm-C biquad with 100MHz center frequency and quality factor 10 was designed as a prototype to confirm with the theoretical design equations. Transistor level circuit implementation of all the analog modules was completed in a standard 0.18 μm CMOS process.