

# ABSTRACT

Design of a Low Power 70MHz-110MHz Harmonic Rejection Filter with Class-AB Output

Stage

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An FM transmitter becomes the new feature in recent portable electronic development. A low power, integrable FM transmitter filter IC is required to meet the demand of FM transmitting feature. A low pass filter using harmonic rejection technique along with a low power class-AB output buffer is designed to meet the current market requirements on the FM transmitter chip. A harmonic rejection filter is designed to filter FM square wave signal from 70MHz to 110MHz into FM sine wave signal. Based on Fourier series, the harmonic rejection technique adds the phase shifted square waves to achieve better THD and less high frequency harmonics. The phase shifting is realized through a frequency divider, and the summation is implemented through a current summation circuit. A RC low pass filter with automatic tuning is designed to further attenuate unwanted harmonics. In this work, the filter's post layout simulation shows -53dB THD and harmonics above 800MHz attenuation of -99dB. The power consumption of the filter is less than 0.7mW. Output buffer stage is implemented through a resistor degenerated transconductor and a class-AB amplifier. Feedforward frequency compensation is applied to compensate the output class-AB stage, which extends the amplifier's operating bandwidth. A fully balanced class-AB driver is proposed to unleash the driving capability of common source output transistors. The output buffer reaches -43dB THD at 110MHz with 0.63V<sub>pp</sub> output swing and drives 1mW into 50 load. The power consumption of the output buffer is 7.25mW. By using harmonic rejection technique, this work realizes the 70MHz-110MHz FM carrier filtering using TSMC 0.18um nominal process. Above 800MHz harmonics are attenuated to below -95dB. With 1.2V supply, the total power consumption including output buffer is 7.95mW. The total die area is 0.946mm<sup>2</sup>.