

ABSTRACT

Power Supply Rejection Improvement Techniques In Low Drop-Out Voltage Regulators

(August 2010)

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Low drop out (LDO) voltage regulators are widely used for post regulating the switching ripples generated by the switched mode power supplies (SMPS). Due to demand for portable applications, industry is pushing for complete system on chip power management solutions. Hence, the switching frequencies of the SMPS are increasing to allow higher level of integration. Therefore, the subsequent post-regulator LDO must have good power supply rejection (PSR) up to switching frequencies of SMPS. Unfortunately, the conventional LDOs have poor PSR at high frequencies. The objective of this research is to develop novel LDO regulators that can achieve good high frequency PSR performance. In this thesis, two PSR improvement methods are presented. The first method proposes a novel power supply noise-cancelling scheme to improve the PSR of an external-capacitor LDO. The proposed power supply noise-cancelling scheme is designed using adaptive power consumption, thereby not degrading the power efficiency of the LDO. The second method proposes a feed forward ripple cancellation technique to improve the PSR of capacitor-less LDO; also a dynamically powered transient improvement scheme has been proposed. The feed forward ripple cancellation is designed by reusing the load transient improvement block, thus achieving the improvement in PSR with no additional power consumption. Both the projects have been designed in TSMC 0.18 μm technology. The first method achieves a PSR of 66 dB up to 1 MHz where as the second method achieves a 55 dB PSR up to 1 MHz.